A New Driving Scheme for Reflective Bistable Cholesteric Liquid Crystal Displays

F. H. Yu and H. S. Kwok*
Center for Display Research and Department of Electrical & Electronic Engineering
Hong Kong University of Science & Technology, Clear Water Bay, Hong Kong

***eekwok@usthk.ust.hk**

Abstract

We investigate a new scheme for driving reflective bistable cholesteric displays. It relies on fast switching from the planar to the focal conic state. We show that 1 ms per line scanning speed is possible using conventional passive matrix drivers. In addition, there is no optical delay in the switching process.

Introduction

A bistable cholesteric display (BCD) exhibits 2 stable states at zero driving voltage: the reflective "planar" P state and the scattering/transparent "focal conic" state. When a dark light absorber is placed at the back of the display, the FC state will appear black and the P state will appear to be bright. The color of the bright state can be adjusted by varying the chirality and pitch of the liquid crystal.

Many schemes have been developed to drive such bistable displays[1-4]. In the conventional scheme of Pfeiffer et al[1,2], commercial STN driver chips were used. A scanning speed of 20 ms per line was achieved. In a more complicated dynamic driving scheme, a 1 ms addressing time was shown to be possible, at the expense of more complicated electronics[3,4]. In both cases, the voltages required were quite high at >40 V.

The dynamic scheme also has the drawback of the appearance of a dark band in the display. Another disadvantage is that the image does not appear instantaneously. There is a 300 ms delay due to the slow switching from the FC state to the P state. Yet, another disadvantage is that the contrast ratio of the dynamic driving scheme is very sensitive to the amplitude of the evolution voltage. Fast switching to the P state has been demonstrated recently in a specially aligned BCD, but it still takes about 10 ms for switching[5].

Here we show results for an improved BCD capable of lower driving voltages and faster switching. We also demonstrate a new driving scheme based on conventional electronics and is capable of 1 ms per line addressing speed. Our scheme is based on the fact that while switching from FC to P takes 0.3 s, switching from the P to the FC takes only 1 ms. The driving scheme is therefore as follows: the whole panel is first set to the P state, then the entire panel is scanned line by line by switching the P state to the FC state only. The voltages are such that the nonselected pixels in the P state will not be affected and will remain in the P state.

In principle, addressing time of <1 ms per line is possible. In our experiment, we demonstrated 1 ms/line, which is already good enough for many applications. The panel writing time is only 0.1 s for a 100 line display. The scanning and data voltages required are also quite low. For our experimental device, the maximum voltage required is 25 V, which can be provided by commercial STN drivers.

Pixel switching characteristics

In order to implement the present scheme, a low voltage cell has to be made. As well, the switching behavior between the P and the FC states has to be studied carefully. Several test cells were made. The cell gaps were 5-um. Special technique was used for homogeneous alignment of the liquid crystal. A mixture of a chiral dopant and ZLI 6204 were used

in the cells. Several different chiral dopants were tested to achieve the best results.

We studied the response of the BCD cell to pulses of various voltages using following procedures: First the cell was driven to the reflective P state (the refresh pulse); then the stabilized reflectance of the cell was measured as a function of the voltage of a switching pulse. This procedure was repeated with the cell in the FC state initially. Both the width of the applied switching pulse and the refresh pulse were 10 ms in this measurement. The pulse duration was changed in other measurements.

In our experiment, the central wavelength of the incident light source was 514 nm. The pitch of the BCD cell was adjusted to match that accordingly. The incident light is near perpendicular to the cell surface.

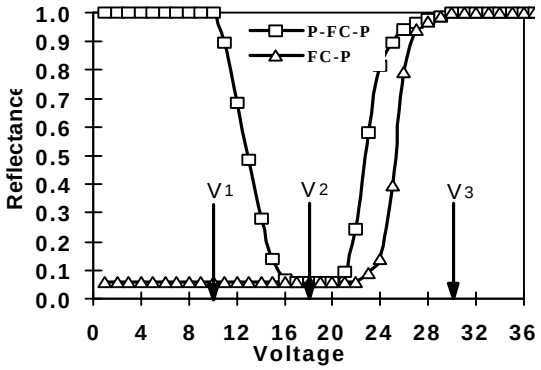

Fig. 1 Reflection of the BCD cell vs the voltage of switching pulse.

The results are shown in Fig. 1, where curve P-FC-P represents the response of the cell originally in the P state prior to the application of the switching pulse. It can be seen that for voltages below 10 V, the reflection is not affected by the switching pulse. When the voltage of the pulse is between 10 V and 16 V, the reflection decreases approximately linearly with increasing voltage. Stable gray scale can therefore be obtained in this region. The reflectance of the cell reaches its original value when the voltage is above 30 V.

Curve FC-P shows the switching behavior of the cell when it was in the FC state prior to the switching pulse. In this case the reflectance of the cell is unchanged by the switching pulse of amplitude below 22 V. The cell is switched to the P state by voltages above 28 V. For both the FC-P and P-FC-P curves, the reflectance contrast between the FC and P states is about 20:1. This value is among the best for the BCD as reported in the literature. Also the voltage values of V_1 = 10 V, V_2 = 18 V and V_3 = 30 V are lower than those reported[1,2].

Figure 2 shows details of the temporal behavior of the switching from the P to the FC state. The upper curve is the applied voltage while the lower curve shows the measured reflectance. From Fig. 2, we find that switching from P to FC occurs early on in the pulse and it is complete in 1 ms.

Even though the switching time in Fig. 2 is shown to be 1 ms, the switching pulse cannot be reduced to 1 ms yet. It was found that if the switching pulse was reduced to 1 ms, the reflectance would rise back up again. A "holding voltage" is needed to stabilize the FC state. In Fig. 2, the holding voltage is provided by the 10 ms switching pulse itself.

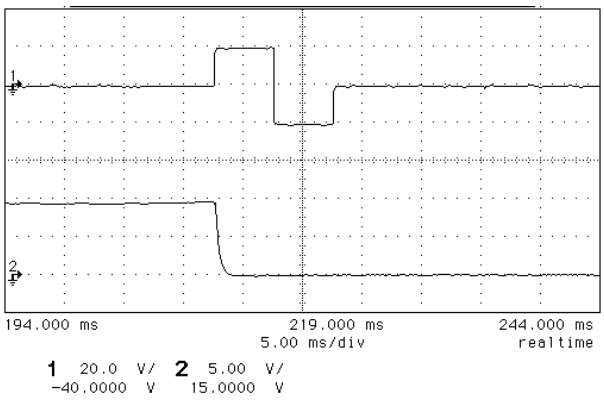

Fig. 2 The switching of the BCD from the P state to FC state. The response time is about 1 ms.

Details of the New Driving Scheme

In our new driving scheme, we rely on the column signal to "hold" the FC state after initial switching by a 1 ms pulse. The idea is that in a multiplex driving scheme, the pixel voltage always consists of the difference between the scanning (row) pulse train and the data (column) pulse train. Hence the pixel voltage will always have a noise-like data pulse train

together with the selection pulse. These data pulses can be used to hold the FC state after switching.

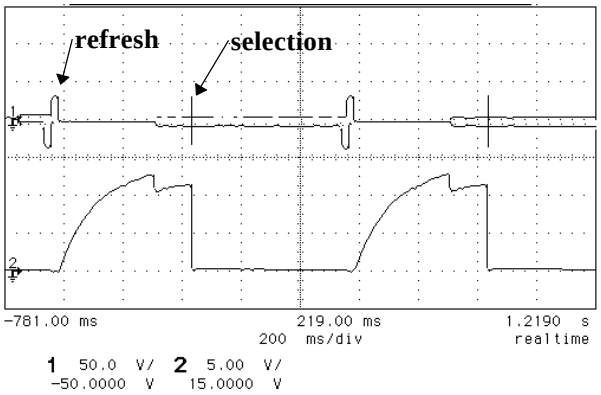

Fig. 3 Switching history between the P and FC states.

Figure 3 shows the reflectance of a simulated "select" pixel with this new scheme. The pixel voltage consists first of the initial 20 ms duration ±30 V refresh pulse which sets the pixel to the P state; then a 1 ms ±30 V switching (selection) pulse sitting on top of a ±6 V background pulse train provides the switching and holding. It can be seen that the switching from P to FC is complete with excellent contrast.

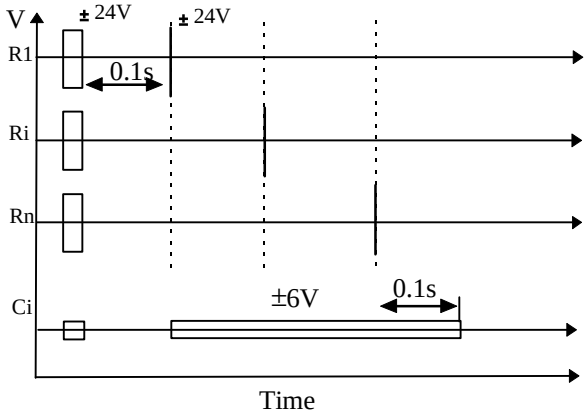

Fig. 4 Timing sequence of the driving scheme. Ri is the row signal and Ci is the column signal.

Fig. 4 shows the new drive scheme for a binary BCD. Grayscale is possible according to Fig. 1 but will not be discussed here. According to this scheme, both the "select" and "nonselect" pixels will see a 10-20 ms ±30 V pulse in the beginning. This pulse refreshes the display to a bright P state. Line-by-line scanning begins after a 0.1 s development time. In the multiplexing scheme, a select pixel will see the sum of the 1 ms address pulse (±24 V) and the data pulse (±6 V). Therefore the "select" pixels will see a ±6 V data train together with a 1 ms ±30 V selection pulse. They will switch to the FC state. In the nonselect pixel, the data pulse reverses sign. Therefore the "nonselect" pixels will see the same data train plus a 1 ms ±18 V pulse. Therefore it is important to make sure that the P state is not affected by this "nonselection" pulse.

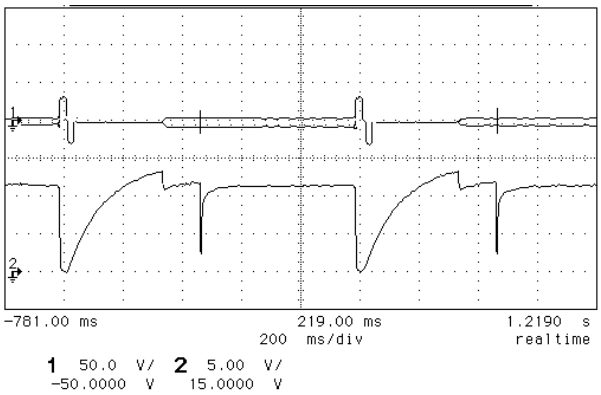

Fig. 5 Influence of the nonselection pulse train on the P state pixel.

Fig. 5 shows the influence of the data pulse train and the 1 ms ±18 V pulse on the P state pixel. It can be seen that the P state remains a P state. The reflectance, however, has decreased by about 15%. This represents basically the cross talk between the select and nonselect pixels. Presumably, further optimization can be performed to reduce this cross talk.

There is a direct correlation between the duration of the switching pulse, i.e. the addressing speed, and the amount of cross talk. For long switching pulses, the voltage required for switching from P to FC can be reduced. Hence the P state will be affected less. We have confirmed this by using 2 ms pulses for switching from P to FC. Experimentally, there was much less cross talk. Hence there has to be a compromise between addressing speed and brightness/contrast of the display. We also have preliminary results showing that the P state is robust against small voltage perturbations occurring during

the scanning with 0.5 ms pulses. But the contrast and brightness are reduced somewhat.

Finally, there are the issues of the holding time and the viewing time in this new addressing scheme. They are both related to the last few lines of the panel. As seen in Fig. 4, a 0.1 s ±6 V pulse train is added at the end of the data pulse train. This is needed to stabilize the FC state for the last few lines of the panel where the 1 ms ±30 V switching pulse appears at the end of the data pulse train. This holding pulse train can be reduced to 0.05s if required.

The viewing time is also needed for the last few lines of the panel. The lower end of the screen are addressed last and pixel selection will appear at a time later than the top of the screen. For a 100 line display, the difference is 0.1s. Therefore, a long viewing time should be allowed between frames in order to equalize the brightness between the top and bottom of the screen. Fortunately, in most applications of BCD, the display does not have to be refreshed frequently. So the difference of 0.1s or even 1s for a 1000 line display is not a big drawback.

Conclusions

In this paper, we demonstrated a new driving scheme for the bistable cholesteric display. This scheme is based on the fast switching from the P to the FC state. Simple voltage pulses as short as 1 ms or shorter can be used to complete this switching, thereby greatly reducing the complexity of the driver electronics.

The present scheme has a comparable addressing speed to the dynamic scheme[3,4]. However, it has the following advantages: (1) Unlike the dynamic scheme, there is no dark band associated with the scanning. The initial refresh pulse produces a bright background which should be more tolerable than a dark band. (2) The driver electronics is much simpler. Conventional driver chips can be used. (3) The voltage requirements are lower. The maximum voltage needed is only 25 V. This should reduce the cost of the driver electronics. (4) Since a majority of the switching is from P to FC, there is no optical delay associated with FC to P switching, which occurs only once per frame in our new scheme.

Bistable cholesteric displays are unique in that once scanned, no refreshing is necessary and the image will stay on. It is well suited for applications in electronic newspaper, pagers, personal data assistants etc. It is believed that the scheme discussed here is a significant improvement over previous schemes and will lead to practical products.

Acknowledgment

This project was supported by the Hong Kong Government Industry Department. Mr. W. C. Yip participated in the early stages of this work.

References

1. D. K. Yang, J. W. Doane, Z. Yaniv and J. Glasser, Cholesteric Reflective Display: Drive Scheme and Contrast, Appl. Phys. Lett., **64**, 1905 (1994).
2. M. Pfeiffer, D. K. Yang, J. W. Doane, R. Bunz, E. Lüder, M. H. Lu, H. Yuan, C. Catchpole and Z. Yaniv, A High Information content Reflective Cholesteric Display, SID 95 Digest, (1995).
3. X. Y. Huang, D. K. Yang, P. J. Bos and J. W. Doane, Dynamic Drive for Bistable Reflective Cholesteric Displays: A Rapid Addressing Scheme, SID 95 Digest, p. 347 (1995).
4. X-Y. Huang, M. Stefanov, D-K. Yang and J. W. Doane, High Performance Dynamic Drive Scheme for Bistable Reflective Cholesteric Displays, SID 96 Digest, p.359, 1996.
5. M. H. Lu, J. Appl. Phys., **81**, 1063 (1997).