Floating low-temperature radio-frequency plasma oxidation of polycrystalline silicon-germanium

Zhineng Fan, Gang Zhao, and Paul K. Chu[a)]
Department of Physics and Materials Science, City University of Hong Kong, Kowloon, Hong Kong

Zhonghe Jin, Hoi S. Kwok, and Man Wong
Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

(Received 26 March 1998; accepted for publication 16 May 1998)

Low temperature oxide formation is an important process in the fabrication of thin-film transistors (TFT) used in active-matrix liquid crystal displays. However, low temperature oxide is prone to have defects at the SiO_2/polycrystalline–SiGe interfaces. We have recently developed a novel rf (radio frequency) plasma oxidation method for polycrystalline SiGe (poly-SiGe) materials. The poly-SiGe wafers are oxidized in an oxygen rf plasma with the samples electrically floating. That is, the sample voltage is the same as the sheath potential of the floating wall and is always negative with respect to the bulk of the plasma since electrons have higher mobility than ions. The slightly negative potential on the wafers attracts low energy oxygen ions from the plasma and the resulting damage on the wafers is thus lower than that induced by the more commonly used and energetic electron cyclotron resonance (ECR) source. No deliberate heating is applied during oxidation since the samples are heated spontaneously by the plasma, but the temperature is measured to be below 100 °C throughout the entire process. The oxidation rate is comparable to that of ECR plasma oxidation. Depth profiles are acquired by Auger electron spectroscopy and the interfaces are examined by x-ray photoelectron spectroscopy. The *n*-channel metal oxide silicon device fabricated on the as-grown gate oxide shows good electrical characteristics. The process is thus compatible with inexpensive large-area, low-temperature fabrication of TFTs on glass substrates. © *1998 American Institute of Physics.* [S0003-6951(98)03629-8]

Low temperature processes are important in the fabrication of thin film transistors (TFTs) used in active-matrix liquid-crystal displays (AMLCD) because the glass substrates cannot tolerate high temperature treatment. Polycrystalline silicon–germanium (poly-SiGe) is more preferable than polycrystalline silicon (poly-Si) in AMLCD because the SiGe film can be deposited and crystallized at lower temperature.[1] However, conventional low-temperature oxide deposition methods give rise to poor porosity, high impurities, and inferior interface quality.[2,3] To improve the quality of the oxide film, plasma-assisted oxidation[4–7] and sputtered oxide[8] have been investigated as alternative methods to synthesize the gate oxide on poly-SiGe and poly-Si TFTs. Results generated from electron cyclotron resonance (ECR) oxidation experiments show that the interfacial defect density is quite high at low temperature, even though a higher temperature alleviates the problem. In this work, we demonstrate a novel approach to grow gate oxide on poly-SiGe materials with low defects at low temperature by floating plasma oxidation using an inductively coupled radio frequency (rf) source.

A 100 nm poly-$Si_{0.8}Ge_{0.2}$ film was deposited in a low-pressure chemical-vapor deposition (LPCVD) system.[9] Oxidation was conducted in a plasma immersion ion implanter utilizing an inductive rf plasma source to generate oxygen plasma surrounding the wafers.[10] To increase the oxidation rate, an aluminum extension was constructed to get the poly-SiGe wafers closer to the source. Figure 1 shows the schematic of the experimental setup. The aluminum sample holder on which the poly-SiGe wafer was placed was positioned 5 cm beneath the rf source. The sample holder was mounted onto the bottom of the vacuum chamber but electrically isolated from the chamber. The instrument was pumped down to a base pressure of 1×10^{-6} Torr before oxygen gas was fed into the chamber. The working pressure was set at 0.1 Torr and the rf power was 900 W. In our experiments, no bias voltage was applied to the sample, and the sample voltage was allowed to float in the oxygen plasma. Since electrons in the plasma move much faster than ions, the potential of the samples is slightly negative relative to the bulk of the plasma. This small potential difference

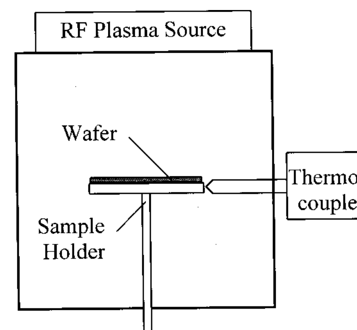

FIG. 1. Schematic diagram of the plasma oxidization setup.

a)Electronic mail: paul.chu@cityu.edu.hk

 © 1998 American Institute of Physics

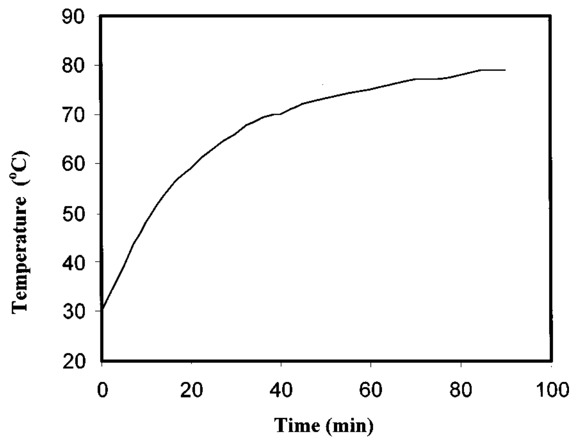

FIG. 2. Variation of sample temperature with oxidation time.

attracts low energy oxygen ions onto the poly-SiGe wafers to carry out the oxidation. Because of its intrinsic low energy nature, the process avoids extensive ion bombardment that induces damage in the wafer and increases the defect density at the SiO_2/SiGe interface.[11,12]

In spite of the lack of external heating, the wafer is heated spontaneously by impinging ions from the plasma during oxidation. To monitor the wafer temperature *in situ*, a thermocouple was installed at the sample stage. Figure 2 depicts the wafer temperature versus oxidation time at 0.1 Torr oxygen and 900 W rf power. The temperature increases rapidly at the beginning of the process. After half an hour, it rises to 65 °C before reaching thermal equilibrium. The final temperature of the 1.5 h process is about 80 °C. It is far below the softening point of the glass substrate and the temperature reached during the other processes. Hence, this oxidation technique is ideal for inexpensive large-area glass substrate circuits.

The oxidized sample grown at 0.1 Torr oxygen plasma for an hour was measured by Auger electron spectroscopy (AES). The substrate is a poly-$Si_{0.8}Ge_{0.2}$ layer on thermal

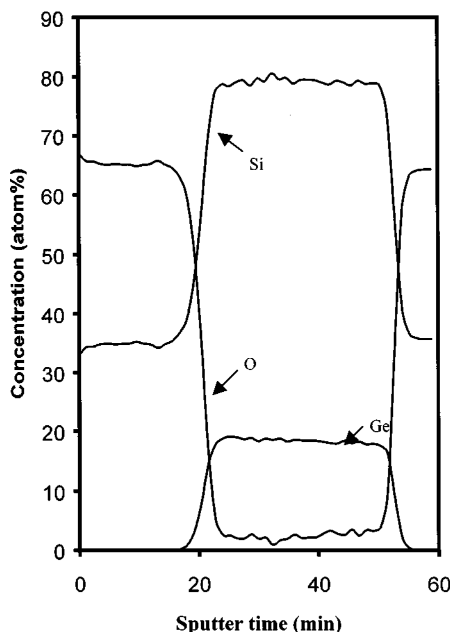

FIG. 3. Auger electron spectroscopy (AES) depth profile of plasma oxidized poly-SiGe.

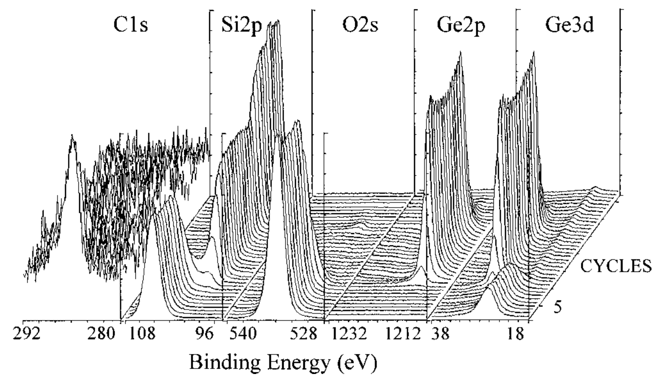

FIG. 4. Stacks of XPS spectra of poly-SiGe with sputtering cycle.

oxide. Figure 3 displays the Ge, Si, and O depth profiles. Comparing the plasma oxidized layer to the thermal oxide layer beneath the poly-SiGe layer, the surface of the poly-SiGe is fully oxidized. The AES results show that the concentration of O in the overlying layer is twice that of Si thereby confirming that stoichiometric SiO_2 has been grown. Very little germanium is detected in this oxide layer (below the AES detection limit which is about 1 at. %) possibly due to the high volatility of GeO_x and Ge segregation out of the stable SiO_2 layer.[13] The interface between the top SiO_2 layer and the poly-SiGe layer is slightly broader than that between the poly-SiGe and thermal oxide, but does not degrade the electrical properties as described later in this article.

Figure 4 depicts a montage of the x-ray photoelectron spectroscopy (XPS) spectra of the plasma-oxidized sample as a function of the sputtering cycle. It can be observed that there is a 4 eV bonding energy shift in the Si-2p peak between the surface oxide layer and the poly-SiGe layer. Both the Ge-2p and Ge-3d peaks terminate at the SiO_2/SiGe interface which is fairly abrupt as the transition only takes two or three cycles as illustrated by the XPS data. This result also confirms that there is no detectable germanium in the oxide layer (<1 at. %), but there is a small accumulation of Ge beneath the oxide/poly-SiGe interface. The peak located at 26 eV is due to O-2s.[5]

To measure the electrical properties, an n-channel metal-oxide-semiconductor (NMOS) transistor with a width to length ratio of 3:2 was fabricated on poly-SiGe oxidized using our floating, low-temperature technique. The substrate

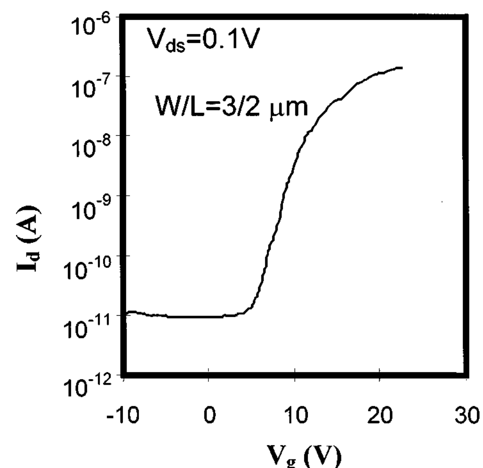

FIG. 5. $I-V$ characteristic of poly-SiGe TFT.

was initially processed in the plasma for 1.5 h at 0.1 Torr. The thickness of the gate oxide was 50 nm. The typical transfer characteristic of the device is exhibited in Fig. 5. It is measured with the drain and source voltage (V_{ds}) fixed at 0.1 V and the body bias left floating. The sub-threshold slope of this device is 2 V/dec. Even though our process is not fully optimized,[13] I_{on}/I_{off} ratios larger than 10^4 can be achieved. The electrical properties of the device fabricated on our as-oxidized wafer are comparable to those of devices processed using LPCVD oxidation at 400 °C.[1,14] It reflects that the defect density at the SiO_2/poly-SiGe interface is similar to that achieved by conventional oxidization processes even though our process is carried out below 100 °C. It is expected that higher performance devices with I_{on}/I_{off} current ratios of 10^6-10^7 can be easily fabricated after hydrogenation.[14–16]

In summary, high quality gate oxide is produced by low temperature (<100 °C) floating rf plasma oxidization on poly-SiGe wafers. The AES and XPS data reveal that stoichiometric SiO_2 can be grown at a rate similar to ECR plasma oxidation in spite of the low temperature. The NMOS device shows good current–voltage characteristics before hydrogenation and its performance is comparable to that of conventionally deposited gate oxide, implying that the interfacial defect density created in our process is quite low. In comparison with ECR oxidation, the floating rf process creates lower damage because the rf plasma is intrinsically less energetic than an ECR plasma. The process is also simpler as it does not require a postannealing step. Our low-temperature oxidation process is thus suitable for inexpensive large-area TFT fabrication.

This work is financially supported by City University of Hong Kong Strategic Grant No. 7000730, and Hong Kong RGC Earmarked Grant Nos. 9040220 and 9040332.

[1] T. J. King, K. C. Saraswat, IEEE Electron Device Lett. **12**, 584 (1991).
[2] A. C. Adams, Semicond. Sci. Technol. **26**, 135 (1983).
[3] W. A. Pliskin, J. Vac. Sci. Technol. **14**, 1064 (1977).
[4] R. K. Chanana, H. A. Upadhyay, R. Dwivedi, and S. K. Srivastava, Solid-State Electron. **38**, 1075 (1995).
[5] P. W. Li, H. K. Liou, E. S. Yang, S. S. Iyer, T. P. Smith III, and Z. Lu, Appl. Phys. Lett. **60**, 3265 (1992).
[6] P. W. Li and E. S. Yang, Appl. Phys. Lett. **63**, 2938 (1993).
[7] I. S. Goh, J. F. Zhang, S. Hall, W. Eccleston, and K. Werner, Semicond. Sci. Technol. **10**, 818 (1995).
[8] Z. Jin. G. A. Bhat, M. Yeung, H. S. Kwok, and M. Wang, Proceedings of the 4th International Display Workshop, Nagoya, Japan, 19–21 November, 1997 (unpublished), p. 239.
[9] Z. Jin. G. A. Bhat, M. Yeung, H. S. Kwok, and M. Wong, IEEE Trans. Electron Devices **44**, 1958 (1997).
[10] P. K. Chu, S. Qin, C. Chan, N. W. Cheung, and P. K. Ko, IEEE Trans. Plasma Sci. **26**, 79 (1998).
[11] K. Lai, K. Kumar, A. Chou, and J. C. Lee, IEEE Electron Device Lett. **17**, 82 (1996).
[12] S. J. Fonash, C. R. Viswanathan, and Y. D. Chan, Semicond. Sci. Technol. **37**, 99 (1994).
[13] P. W. Li, E. S. Yang, Y. F. Yang, J. O. Chu and B. S. Meyerson, IEEE Electron Device Lett. **15**, 402 (1994).
[14] T. J. King and K. C. Saraswat, IEEE Trans. Electron Devices **41**, 1581 (1994).
[15] S. Qin, Y. Zhou, T. Nakatsugawa, and C. Chan, Nucl. Instrum. Methods Phys. Res. B **124**, 69 (1997).
[16] Y. S. Kim, K. Y. Choi, S. K. Lee, and B. H. Min, Jpn. J. Appl. Phys. Part 1 **33**, 649 (1994).