High Performance Polycrystalline SiGe Thin Film Transistors Using Al_2O_3 Gate Insulator

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Abstract

The use of aluminum oxide as the gate insulator for low temperature (<600°C) polycrystalline SiGe thin film transistors (TFTs) has been studied. The aluminum oxide was sputtered from a pure aluminum target using a reactive N_20 plasma. The composition of the deposited aluminum oxide was found to be almost stoichiomertic (i.e. Al_2O_3), with a very small fraction of nitrogen incorporation. Even without any hydrogen passivation, good TFT performance was measured on devices with 50nm thick Al_2O_3 gate dielectric layers. Typically, a field effect mobility of 47cm^2/Vs, a threshold voltage of 3V, a sub-threshold slope of 0.44V/decade, and an on/off ratio above 3×10^5 at a drain voltage of 0.1V can be obtained. These results indicate that the native interface between the Al_2O_3 and the SiGe channel layer is sufficiently passivated to make Al_2O_3 a better alternative to grown or deposited SiO_2 for SiGe field effect devices.

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Introduction

SiGe has been proposed as an attractive alternative to Si in a variety of micro-electronic applications. In bipolar transistors, it has been used to form narrow bandgap base regions [1]. In field effect devices, it has been used to form midgap gate electrodes [2]. In large area electronics such as flat panel displays, its potential advantages include higher mobility and lower solid state crystallization (SPC) temperature [3]. In all of these applications, the processing of SiGe is believed to be "compatible" to the processing of Si. However, because of the poor interface between a conventional SiO_2 gate insulator and the polycrystalline SiGe (poly-SiGe) channel layer, there is still significant disparity, particularly for NMOS TFTs, between the best reported performance of poly-SiGe and that of poly-Si TFTs, even after extensive hydrogenation. Clearly, improvement of the interface quality holds the key to realizing better performing poly-SiGe TFTs.

A possible approach to improving the interface quality is to use alternative techniques of gate insulator formation. Low temperature electron cyclotron resonance grown SiO_2 [4] and sputtered oxide [5] have been investigated with some degrees of success. Yet a different approach is the use of alternative gate dielectric materials. Since Al_2O_3 has been used as part of the gate insulators of amorphous Si TFTs [6], its applicability in poly-SiGe is investigated in this work.

Experimental

The Al_2O_3 thin films used in this work were formed in a novel RF plasma reactive sputtering deposition system, a schematic of which is shown in Figure 1. The Al target and the wafer chuck form the parallel plate electrodes for the plasma. The diameters of the target and the wafer chuck are about 5cm. The pressure in the vacuum chamber was controlled by a butterfly valve and the gas flow rate. An 18.7kHz RF power generator was used to generate the plasma. Al_2O_3 was sputtered reactively using an N_2O plasma, with the wafer temperature controlled by an electrical heater underneath the wafer chuck. Relevant process conditions are summarized in Table 1.

A depth profile (Figure 2) of the atomic concentration of various elements within an Al_2O_3 layer in its as-deposited form has been obtained using X-ray photo-electron spectroscopy (XPS). The thickness of the film is about 50nm and the ratio of aluminum to oxygen is around 2 to 3 with a small but non-negligible nitrogen content.

This indicates the film is largely stoichiometric. The Al2p binding energy of 76.4eV shown in the XPS spectrum in Figure 3 provides further proof of the full oxidation of Al.

NMOS poly-SiGe TFTs were fabricated using a conventional 4-mask self-aligned process with a maximum processing temperature of no greater than 600°C. The process began with 100mm, (100)-oriented N-type Si wafers with 500nm of thermally grown oxide. A 100nm thick layer of SiGe was deposited in a low pressure chemical vapor deposition (LPCVD) system [7] to form the channel layer. Silane and germane at respective flow rates of 100sccm and 10sccm were used as the source gases. The deposition temperature was 550°C. The Ge content in the deposited SiGe films was 15%, measured using Rutherford back-scattering spectroscopy. X-ray diffraction analyses indicated that the as-deposited films were polycrystalline. Following the deposition of the channel layer and transistor island patterning by plasma etching, the wafers were cleaned and loaded in the reactive sputtering system for Al_2O_3 deposition. The thickness of the film was adjusted by controlling the deposition time and checked using a surface profilometer. The gate electrodes were realized by patterning 280nm thick LPCVD $Si_{0.55}Ge_{0.45}$ thin films. The Al_2O_3 not covered by the gate electrode was etched in a buffered HF solution. The source, the drain and the gate regions were doped by a self-aligned $4x10^{15}/cm^2$ phosphorus implantation. Before the 5-hour implant activation at 600°C, a 500nm thick chemical vapor deposited low temperature oxide (LTO) pre-metal insulation layer was laid down, using SiH_4 and O_2 at 425°C. Subsequently, the contact holes were opened in a buffered HF solution and 1µm of Al-Si1% was sputter deposited. Finally, the devices were sintered in Forming gas for 30 minutes at 400°C. No plasma hydrogenation was performed, so that the “intrinsic” performance of the devices can be measured.

Results and discussions

The fabricated devices were characterized using an HP4156 Precision Semiconductor Parameter Analyzer. Typical room temperature IV curves of the poly-$Si_{0.85}Ge_{0.15}$ TFTs and the corresponding gate leakage current are shown in Figure 4. Though a soft increase in the gate leakage occurred at around 4.5V, it is low during all the measurements. Such leakage can be reduced either by optimizing the deposition or

the annealing condition of the reactively sputtered Al_2O_3 film or by capping it with a thin layer of LTO. The drain current (I_d) begins to increase rapidly at a gate voltage (V_g) of 1V and quickly enters the linear regime at about 3V, indicating a very effective gate control. The estimated threshold voltage and the sub-threshold slope are 3V and 0.44V/decade, respectively. At a drain voltage (V_{ds}) of 0.1V, the off current is lower than 1pA/µm. This translates to an on/off ratio of greater than 3×10^5, even without any deliberate hydrogen passivation. A field-effect mobility (μ_{FE}) of 47cm^2/Vs can estimated using the following equation:

$$\mu_{FE} = \frac{1}{V_d}\frac{L}{W}\frac{1}{C_{ox}}\frac{\mathrm{d}I_d}{\mathrm{d}V_g},$$

where L is the channel length, W the channel width, and C_{ox} the capacitance per unit area of the 50nm Al_2O_3. A dielectric constant of 10 was assumed for Al_2O_3. This mobility is much better than that of the poly-SiGe TFTs using SiO_2 as the gate insulators [3,8,9].

The I_d-V_d curves are shown in Figure 5. The behavior is typical of field effect TFTs showing partial saturation effects at high V_d. The slight increase of I_d at V_d above 4.5V is probably caused by grain boundary enhanced “kink” effects.

The performance of the device shown in Figures 4 and 5 is much better than similar devices realized with SiO_2 as the gate insulators. A comparison of the relevant parameters is summarized in Table 2. The good sub-threshold slope obtained in this work is better than those obtained on heavily hydrogenated devices with SiO_2 gate insulators. Part of this improvement resulted from the higher dielectric constant of Al_2O_3, which is about 2.5 times that of SiO_2. A more important reason is the improved interface between the Al_2O_3 dielectric and the SiGe channel layer. The mobility obtained in this work is comparable to state-of-art poly-Si devices, this is the first time ever that high mobility poly-SiGe TFTs have been realized without extensive hydrogenation. This makes the Al_2O_3 a significantly better substitute for SiO_2 as the gate insulators for poly-SiGe TFTs.

As shown in Figure 2, the Al_2O_3 contains about 5% of nitrogen. This is because N_2O was use as the reaction gas instead of pure O_2. At the present moment, it is not clear whether the nitrogen plays an active role in improving the interface quality.

Experiments are planned to clarify this ambiguity and improve the breakdown voltage of the material.

Conclusion

A novel reactive sputter deposition system was used to form Al_2O_3 as the gate insulators of poly-SiGe TFTs. Material analyses indicate the deposited film is largely stoichiometric, with about 5% nitrogen incorporation. Devices with 50nm thick Al_2O_3 gate insulators were fabricated at temperatures not exceeding 600^oC. The fabricated devices showed excellent performance even without any deliberate hydrogenation. Compared to poly-SiGe TFTs with SiO_2 as gate insulators, the field-effect mobility and the sub-threshold slope improved significantly, indicating a good interface between Al_2O_3 and the SiGe channel layer. These results suggest that Al_2O_3 is more suitable than SiO_2 as a gate insulator material for poly-SiGe TFTs.

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Figure 5: I_d-V_d curve of the poly-SiGe TFT with 50nm Al_2O_3 gate insulator.

Table 1.

RF power	450W
RF frequency	18.7kHz
N_2O flow rate	400sccm
Chamber pressure	200 mTorr
Substrate temperature	380^oC
Deposition time	85 minutes

Table 2.

	Before Hydrogenation		After Hydrogenation	
	Al_2O_3	SiO_2 [Ref.3][*1]	SiO_2 [Ref. 9][*2]	SiO_2 [Ref. 8][*3]
Field effect mobility (cm^2/Vs)	47	0.1	2.2	38
Threshold voltage (V)	3	13.6	19.5	5.5
Sub-threshold slope (V/decade)	0.44	2.0	4.3	1.5
On/off ratio	$2x10^5$	500	Not available	$>1\ x10^6$

*1. Fabricated with a 550°C SPC process.
*2. Passivated by hydrogen implantation.
*3. Passivated in hydrogen plasma

Fig. 1

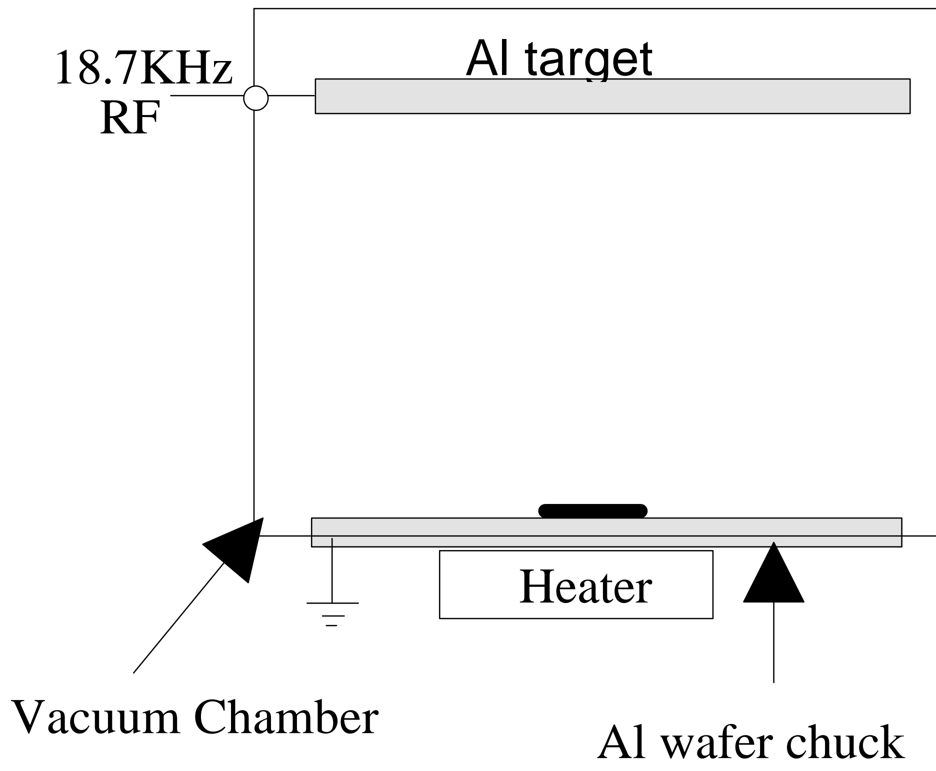

Fig. 2

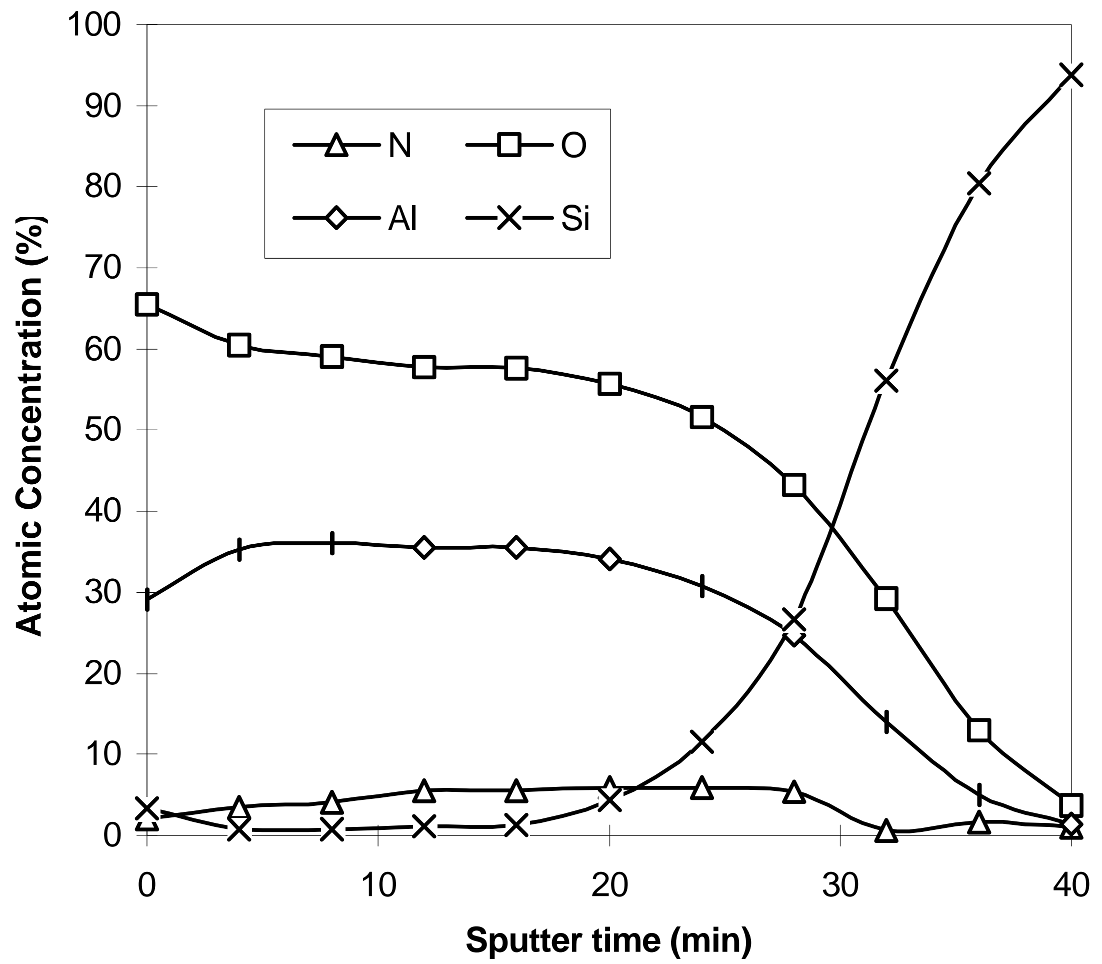

Fig. 3

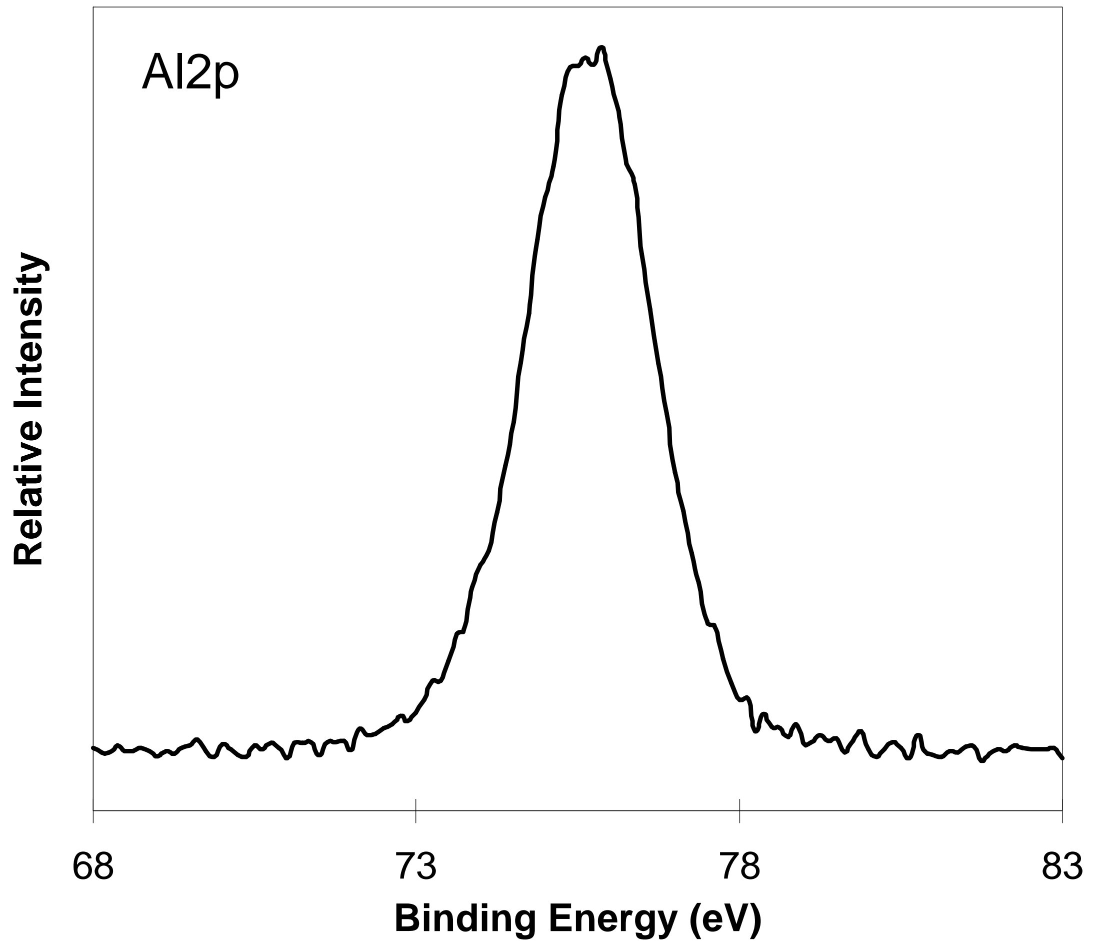

Fig. 4

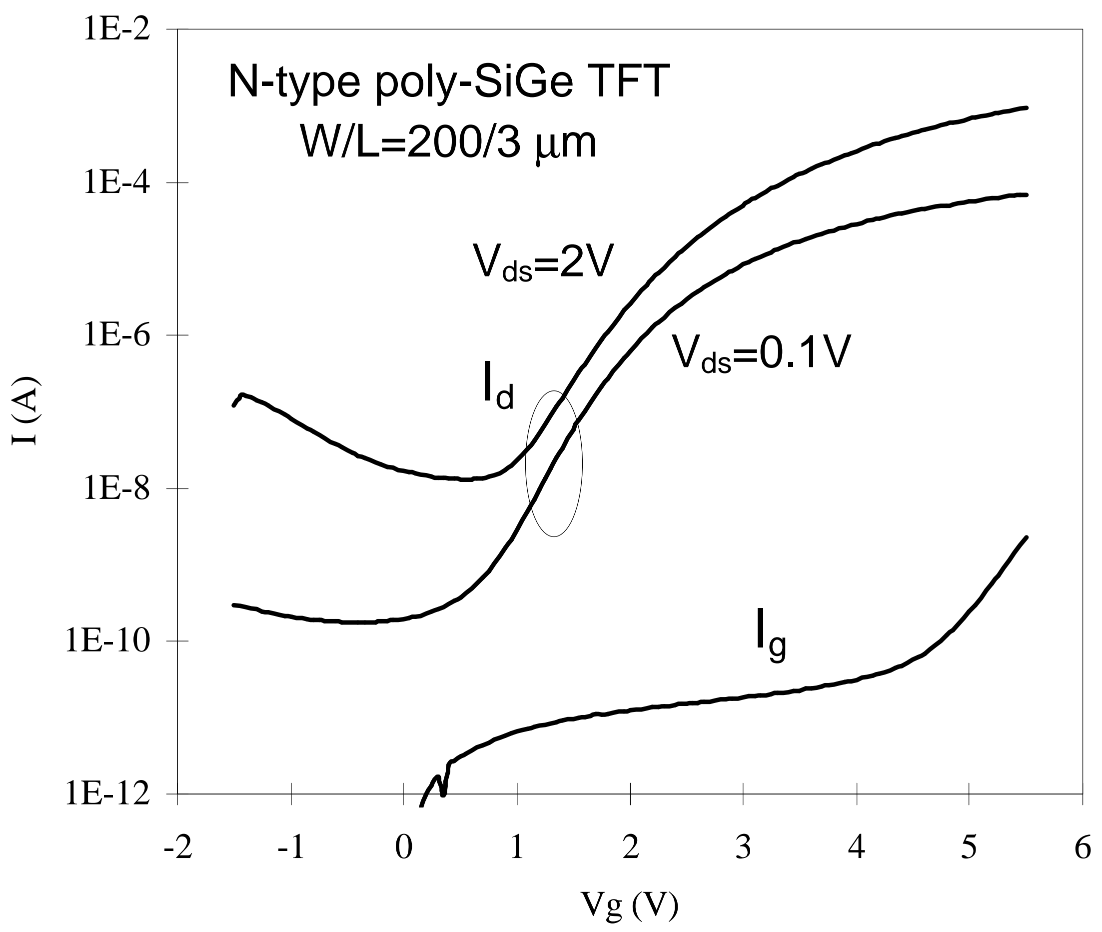

Fig. 5