Effects of Longitudinal Grain Boundaries on the Performance of MILC-TFT's

Gururaj A. Bhat, Zhonghe Jin, Hoi S. Kwok, and Man Wong

***Abstract*— Compared to conventional solid phase crystallized (SPC) thin-film transistors (TFT's), metal induced laterally crystallized (MILC) TFT's exhibit significantly enhanced performance at reduced processing temperature. It is concluded that the major improvements in MILC-TFT's result from the growth of the crystal grains in a direction longitudinal to that of the current flow, whereas in SPC-TFT's, the grain boundaries are randomly oriented. It is also observed in this work that while the MILC-TFT's are less sensitive to short-channel effects (SCE's), their leakage current exhibits higher sensitivity to channel length reduction. These differences again can be traced to the different arrangements of the grain boundaries in the two types of devices.**

***Index Terms*—Lateral crystallization, MMGB, nickel, thin-film transistors.**

I. Introduction

HIGH-MOBILITY polycrystalline silicon (poly-Si) thin-film transistors (TFT's) with low leakage currents are desirable for integrating driver circuits and pixel transistors on the same glass panel for liquid crystal displays (LCD's). The replacement of amorphous Si (a-Si) by poly-Si in the pixel array offers many advantages [1]. Among other things, process complexity is reduced by eliminating potentially conflicting requirements for the fabrication of poly-Si and a-Si devices and equivalent magnitudes of drive current can be realized with smaller poly-Si TFT's, thus increasing the aperture ratio in the displays. The main obstacle against a wider application of poly-Si TFT's is its relatively high processing temperature, which exceeds the upper processing temperature limit of the inexpensive glass substrates for LCD's.

Large grained poly-Si can be obtained using a variety of techniques: rapid thermal annealing (RTA) [2], excimer laser crystallization (ELC) [3], and SPC [4]. RTA is a high-temperature (>600 °C) process and the resulting films contain high densities of defects. By localizing the high temperature to the silicon layer, ELC can be considered a "low" temperature process. While it is capable of producing poly-Si films with low defect densities, it suffers from high initial cost and high process complexity. Conventional SPC is a relatively inexpensive batch process, though at around 600 °C, the processing temperature is still considered high. Recently, a low-temperature (∼500 °C) variant of SPC using MILC has been proposed [5]. While still high compared to that of ELC, the lower processing temperature (500 °C) of MILC should produce less glass shrinkage compared to the 600 °C SPC processes.

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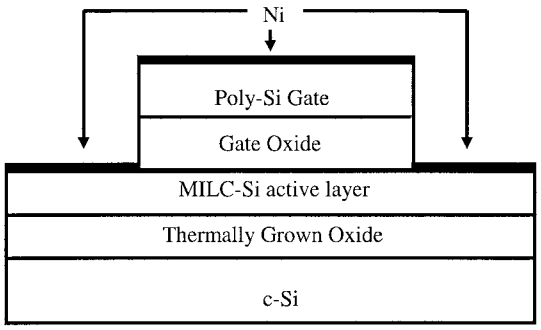
II. Device Fabrication

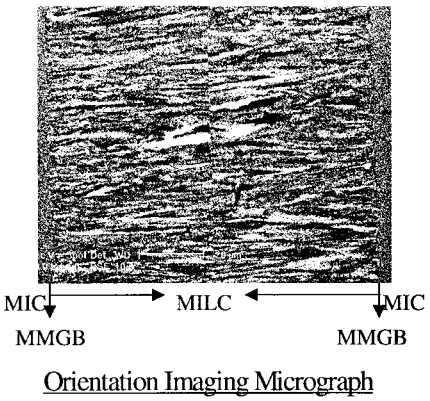
Four-in silicon wafers covered with 100-nm-thick thermal oxide were used as the starting substrates. A thin 100-nm a-Si layer was first deposited by low-pressure chemical vapor deposition (LPCVD) at respective pressure and temperature of 300 mtorr and 550 °C. After patterning the a-Si layer to form the active islands, a 100-nm thick layer of low-temperature oxide (LTO) gate insulator and 200-nm thick a-Si layer gate electrode were deposited. The wafers were thoroughly cleaned after the gate patterning and the exposure of the source and drain regions. About 2 nm of Ni metal was evaporated in an ultrahigh vacuum system, before the source, drain, and gate regions were doped by self-aligned phosphorus implantation at a dose of $3\times 10^{15}/\text{cm}^2$ and energy of 40 keV. Subsequently, the devices were heat-treated at 500 °C for 9 h, during which Ni induced crystallization of the a-Si layer was accomplished and the dopants activated. No attempt was made to remove any remaining Ni metal after the MILC. Finally, contact patterning and Al-1% Si sputtering was followed by sintering in Forming gas at 400 °C for 30 min. For comparison, devices were also fabricated using SPC at 625 °C for 10 h. The schematics of the devices are shown in Fig. 1(a).

III. Device Characterization

Devices with channel lengths down to 2 μm were characterized using an HP4156A Semiconductor Parameter Analyzer. The threshold voltages (V_t) of the devices were defined as the gate voltages (V_g) required to achieve a normalized drain current (I_d) of $(W/L)\times 10$ nA, where W and L are the channel width and length, respectively. The field effect mobility (μ_{FE}) was extracted from the maximum transconductance $(g_{\max})$. As verified by the current–voltage (I–V) curves presented in Fig. 2, the performance of the MILC-TFT's is indeed far superior to that of the SPC-TFT's fabricated under the same conditions which are not the optimum conditions for SPC-TFT's. A comparison of the relevant device parameters of the two kinds of devices is summarized in Table I. Clearly, the MILC-TFT's have lower V_t, smaller subthreshold slope (S), and higher μ_{FE}.



(a)



(b)

Fig. 1. (a) Schematic of MILC-TFT structure. (b) SEM micrograph showing longitudinal grains, grain boundaries, and conceptual potential barrier formation across grain boundaries in MILC-TFT and SPC-TFT.

It is well known that SPC poly-Si has a columnar grain structure with grain boundaries randomly oriented with respect to the direction of I_d [7]. These grain boundaries trap charge carriers and build up potential barriers to the flow of carriers. The presence of the potential barriers and the additional scattering at the grain boundaries result in $\mu_{\rm FE}$ degradation. The high density of trap states deteriorates S and increases V_t. These problems are alleviated in MILC-TFT's because, as depicted in Fig. 1(b) consisting of SEM micrograph and potential barriers formation across the grain boundaries, the longitudinal grains and their boundaries (LGGB's) are largely parallel to I_d–hence less impeding to carrier flow and resulting in lower V_t, smaller S, and higher $\mu_{\rm FE}$. This explains the faster turn-on and the higher on-current (Fig. 2) for the MILC-TFT's.

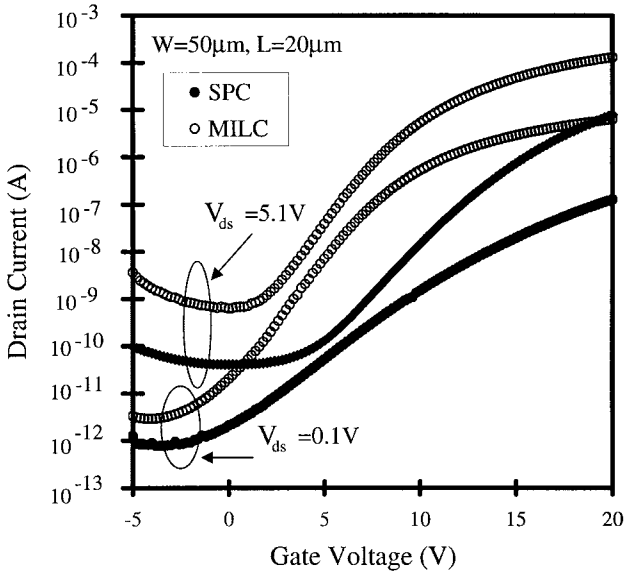


Fig. 2. Transfer characteristics of MILC-TFT and PSC-TFT.

TABLE I
COMPARISON OF THE RELEVANT DEVICE PARAMETERS OF MILC-TFT AND SPC-TFT's

	V_t (V)	S (V/dec)	I_{min} (pA)	μ_{FE} (cm^2/Vs)
MILC-TFT	6.2	1.2	2.9	74
SPC-TFT	15.6	3.3	0.8	5

IV. Comparison of Short-Channel Effects

Short-channel effects (SCE's), indicated by V_t roll-off with L, as shown in Fig. 3, commence at about $L = 10$ μm in SPC-TFT's, significantly longer than that of 5 μm observed in MILC-TFT's. This is very desirable from a scaling point of view: devices can be made smaller to further improve aperture ratio and operating speed.

In SPC-TFT's, some of the grain boundaries and potential barriers are transverse to I_d, hence their associated electric field is parallel to the length of the channel. It is obvious that this electric field adds to the drain bias and causes an earlier on-set of SCE's in SPC-TFT's, when compared to their single crystal counterpart [8]. In MILC-TFT's, the LGGB's are largely parallel to the length of the channel. The enhancement of drain field penetration by the grain boundary electric field is significantly reduced, hence reduced SCE's are observed.

V. Comparison of Leakage Current

The leakage current and its sensitivity to L (Fig. 4) have been measured for both MILC- and SPC-TFT's. Consistent with previously reported result [9], the leakage current of MILC-TFT's was generally higher than that of SPC-TFT's. Moreover, our results also indicates that the leakage current of MILC-TFT's is significantly more sensitive to reduction in L than that of SPC-TFT's.

The presence of grain boundaries and intragrain trap states are responsible for enhanced leakage current in poly-Si TFT's. Depending on the nature of the trap states and the biasing

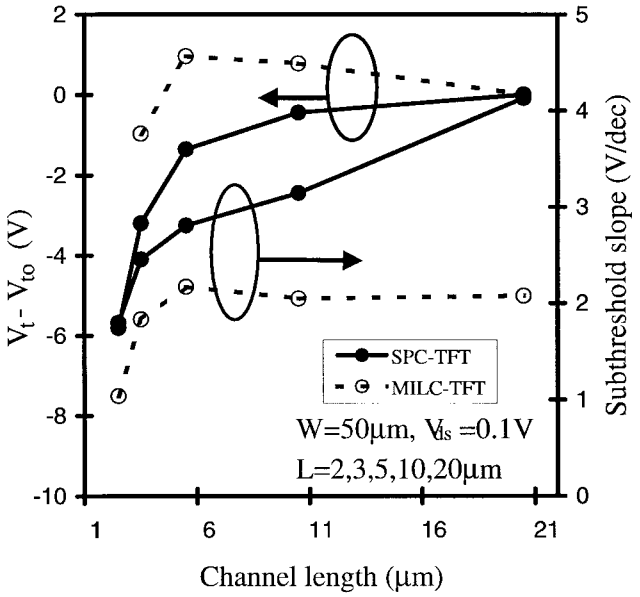


Fig. 3. Dependence of V_t and S on L for MILC-TFT and SPC-TFT. $V_{\rm to}$ is the threshold voltage of the device with the longest channel length.

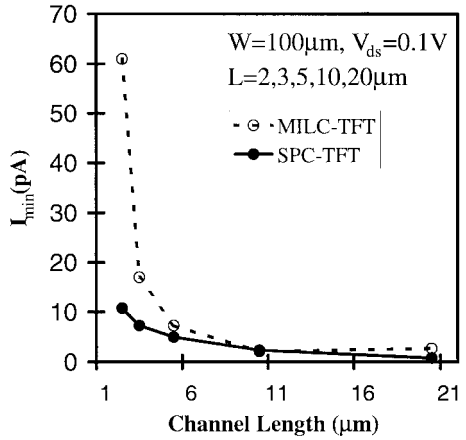


Fig. 4. $I_{\rm min}$ versus channel length for N-channel MILC-TFT and SPC-TFT.

conditions, leakage current is enhanced due to one or a combination of emission mechanisms [10]. At low drain and gate bias, trap assisted thermionic emission is the dominant leakage mechanism [11]. In single crystal or SPC devices, metal precipitate induced traps have not been considered for obvious reasons. However, in MILC-TFT's, Ni is used to induce the crystallization of a-Si. It is inevitable that small amounts of Ni or $NiSi_2$ precipitates are present and further enhance the leakage current [9], [12].

It is possible to consider the total resistance to the flow of leakage current as composing of two components: channel resistance and junction resistance. Clearly the channel resistance scales with L, hence the leakage current increases with reduced channel length. This has been observed in both SPC- and MILC-TFT's. However, at sufficiently reduced L, the junction resistance may become dominant. If the behavior of the junctions in MILC- and SPC-TFT's is different, different sensitivities to L (Fig. 4) in the two kinds of devices will be observed. It is clearly implied from the measured leakage current data that the I–V characteristics of the junction in MILC-TFT's is highly nonlinear and show "diode"-like rapid turn on at some applied voltage.

From a microstructural point of view, there is evidence from transmission electron microscopy [13] showing that a distinct grain boundary exists at the intersection of the metal-induced-crystallization (MIC) and the MILC regions. In the MILC-TFT's realized in this work using a conventional process [5], such MIC/MILC grain boundaries (MMGB's), which contain trapped Ni or $NiSi_2$, coincide with the source and drain metallurgical junctions, hence located inside the corresponding depletion regions. This is unlike in SPC-TFT's, in which grain boundaries are randomly distributed and may or may not exist in the source and drain junctions. It is most likely that this is responsible for the different sensitivity of the leakage current to L in the MILC- and SPC-devices.

VI. Conclusion

Compared to SPC-TFT's, the improvements in device performance in MILC-TFT's is predominantly due to the LGGB's. Reduced sensitivity to SCE's makes MILC-TFT's more scalable. The reason behind the enhanced leakage current MILC-TFT's could be the nonlinearity associated with the junction resistance. This nonlinearity may arise from the overlap of the metallurgical junctions with the MMGB's.

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