Characteristics of P- and N-Channel Poly-Si/$Si_{1-x}Ge_x$/Si Sandwiched Conductivity Modulated Thin-Film Transistors

Chunxiang Zhu, *Student Member, IEEE*, Johnny K. O. Sin, *Senior Member, IEEE*, and Hoi-Sing Kwok

***Abstract*—Both p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched conductivity modulated thin-film transistors (CMTFTs) are demonstrated and experimentally characterized. The transistors use a poly-Si/$Si_{1-x}Ge_x$/Si sandwiched structure as the active layer to avoid the poor interface between the gate oxide and the poly-$Si_{1-x}Ge_x$ material. Also an offset region placed between the channel and the drain is used to reduce the leakage current. Furthermore, the concept of conductivity modulation in the offset region is used to provide a high on-state current. Results show that the transistors provide a high on-state current as well as a low leakage current compared to those of conventional offset drain TFTs. The p- and n-channel CMTFTs can be combined to form CMOS drivers, which are very suitable for use in low temperature large area electronic systems on glass applications.**

***Index Terms*—CMOS, CMTFT, conductivity modulation, poly SiGe, thin-film transistor.**

I. Introduction

LOW TEMPERATURE polysilicon TFT (thin-film transistor) appears to be one of the most promising technologies for the ultimate goal of building large area electronic systems on glass substrates [1]. In flat panel liquid crystals, electroluminescent, and plasma displays as well as other applications such as high speed printers and page width optical scanners, etc., poly-Si TFT can be used to integrate peripheral driver circuits on glass for system integration [2]. This integration greatly reduces the number of external connections as well as the number of driver chips, resulting in a lower cost and improved reliability [3].

Due to the lower thermal budget and higher mobility, polycrystalline silicon-germanium (poly-$Si_{1-x}Ge_x$) has been investigated recently as an alternative to polysilicon for TFT applications [4]–[6]. However, due to the poor interface between the poly-$Si_{1-x}Ge_x$ channel and the SiO_2 gate dielectric, devices with relatively poor on-state and leakage performance compared to polysilicon devices were obtained. To alleviate this problem, a top thin layer of poly-Si is introduced to avoid the poor interface between the poly-$Si_{1-x}Ge_x$ and the gate oxide [7], [8]. However, the leakage current of the devices was still high compared to that of the poly-Si counterpart due to the fact that the poly-$Si_{1-x}Ge_x$ active layer used has a smaller band gap [8].

In this paper, both p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched conductivity modulated thin-film transistors (CMTFTs) [10]–[12] are demonstrated and characterized. The transistors use a poly-Si/$Si_{1-x}Ge_x$/Si sandwiched structure as the active layer to avoid the poor interface between the gate oxide and the poly-$Si_{1-x}Ge_x$ material. Also, an offset region placed between the channel and the drain is used to reduce the leakage current. Furthermore, to provide a high on-state current, the concept of conductivity modulation in the offset region is used. The fabrication process, the on-state/off-state current–voltage (*I–V*) characteristics, and the breakdown performance of these devices will also be discussed.

II. Device Structure and Operation

To demonstrate the superior performance of the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched CMTFTs, both the p- and n-channel conventional offset drain TFTs and CMTFTs were fabricated on the same substrate for comparison using a low temperature process ($\leq$600 °C). Schematic cross sections of the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si conventional offset drain TFT and CMTFT are shown in Fig. 1(a) and (b). All devices used a poly-Si/$Si_{1-x}Ge_x$/Si sandwiched structure as the active layer. The poly-Si layer at the bottom was used to avoid the problem of poor nucleation of the $Si_{1-x}Ge_x$ film placed directly onto the SiO_2. The top poly-Si film was introduced to avoid the poor interface between the poly-$Si_{1-x}Ge_x$ and the SiO_2 gate dielectric. For the p-channel devices, due to the band discontinuity in the valence band, holes are confined in the poly-$Si_{1-x}Ge_x$ film. Thus, the devices provide high hole mobility in the poly-$Si_{1-x}Ge_x$ film. Furthermore, introduction of the top poly-Si film will reduce the scattering due to the good interface between the poly-Si and poly-$Si_{1-x}Ge_x$layers, which enhances the mobility further. However, in the case of the n-channel devices, due to the very small conduction band offset, the channel will be formed at the top (50 Å) of the poly-Si film (the order of the thickness of the inversion charge). Fortunately, the electron mobility in the poly-Si is very close to that in the poly-$Si_{1-x}Ge_x$ [9].

The conventional offset drain TFT is a majority carrier device and has a lightly doped offset region placed between the channel and the drain for the low leakage current. In addition to the introduction of the offset region, the CMTFT uses the concept of conductivity modulation. In the case of the p-channel CMTFT,

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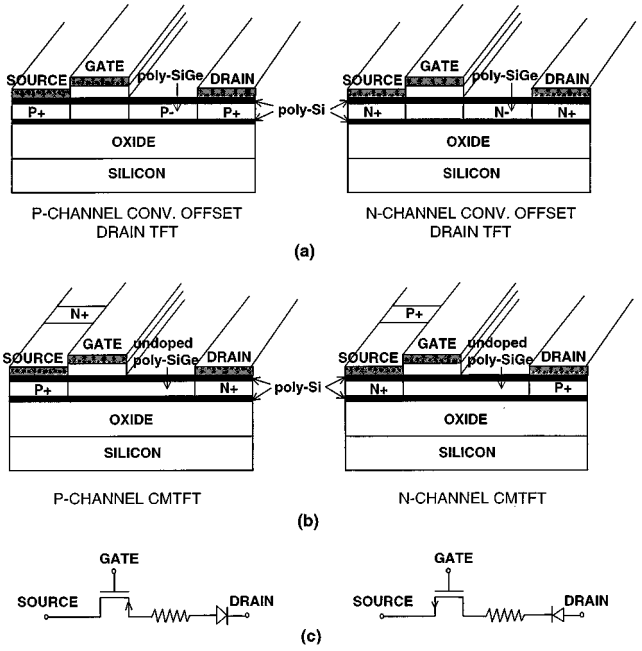

Fig. 1. Schematic cross section of the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si (a) conventional offset drain TFTs, (b) CMTFTs, and (c) the equivalent circuit model for Fig. 1(b).

an n^+ drain region is incorporated instead of a p^+ drain region used in the p-channel conventional offset drain TFT. The offset and drain regions can be viewed as a series combination of a diode and a drift resistance as shown in Fig. 1(c). When the gate voltage is above the threshold voltage and the drain voltage is high enough, the drain diode is turned on, and electrons are injected into the offset region from the n^+ drain. The injected electrons recombine with the traps associated with the grain boundaries and facilitate the flow of holes in the offset region. The high concentration of injected electrons conductivity modulates the resistivity of the offset region and reduces the on-state resistance dramatically compared to that of the conventional offset drain TFT, resulting in a high on-state current. In order to prevent minority carrier accumulation in the channel region, a segmented source structure with a 10 : 1 segmentation ratio (a ratio of the layout dimensions of the p^+ region to n^+ region) is used as shown in Fig. 1(b). For the n-channel devices, all the p-type regions are replaced by n-type regions and vice versa.

In contrast to the conventional offset drain TFT in which a lightly doped offset region is used, the CMTFT uses an undoped offset region. The breakdown voltage of the CMTFT is therefore dependent on the channel length and offset region length. At zero gate voltage, the large drain voltage is blocked by the intrinsic region between the source and drain regions.

III. Device Fabrication

The major fabrication steps of the p-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT are shown in Fig. 2. The fabrication process for the n-channel devices is the same as that for the p-channel but with the p-type and n-type dopant interchanged. Silicon wafers with a thermally grown oxide layer of 5000 Å were used as starting substrate. First, a thin layer

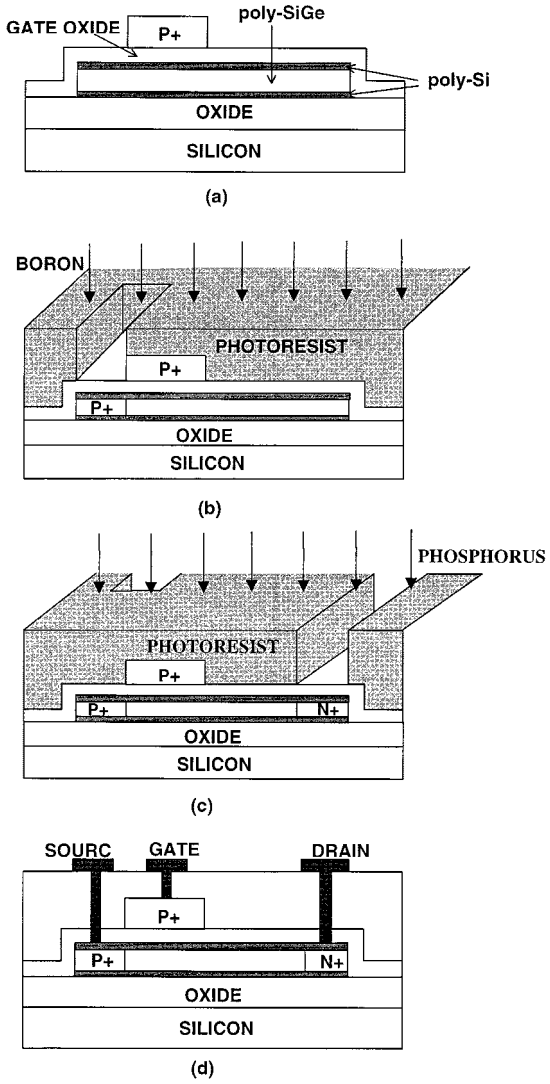

Fig. 2. Major fabrication steps of the p-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT.

of amorphous Si (α-Si) was deposited as seeding layer. Then a 2000 Å thick layer of α-$Si_{1-x}Ge_x$ was deposited at 500 °C with a 150 sccm flow rate of SiH_4 and an 8 sccm flow rate of GeH_4. The composition of Ge is 10%. A higher concentration of Ge will cause the leakage current to be higher. Finally, a 50 Å of α-Si was deposited on the $Si_{0.9}Ge_{0.1}$. All the layers were deposited with LPCVD. The sandwiched structure was then recrystallized to polycrystalline form by furnace annealing at 600 °C in nitrogen ambient for 20 h. Afterward, the device islands were defined by plasma dry etching. In the case of the p-channel conventional offset drain TFT, a boron implant with a dose of 1×10^{12} cm^{-2} was used to dope the offset region. After that, a 1000 Å layer of oxide was deposited as the gate oxide using APCVD. The gate polysilicon layer was then deposited at 600 °C using LPCVD with a target thickness of 2500 Å. It was then implanted with boron at a dose of 4×10^{15} cm^{-2} and energy of 33 keV and patterned. The source was doped by a 33 keV boron implant with a dose of 4×10^{15} cm^{-2}. The drain was doped by a 40 keV phosphorus implant with a dose of 5×10^{15} cm^{-2}. After the source and drain implantation, 3500

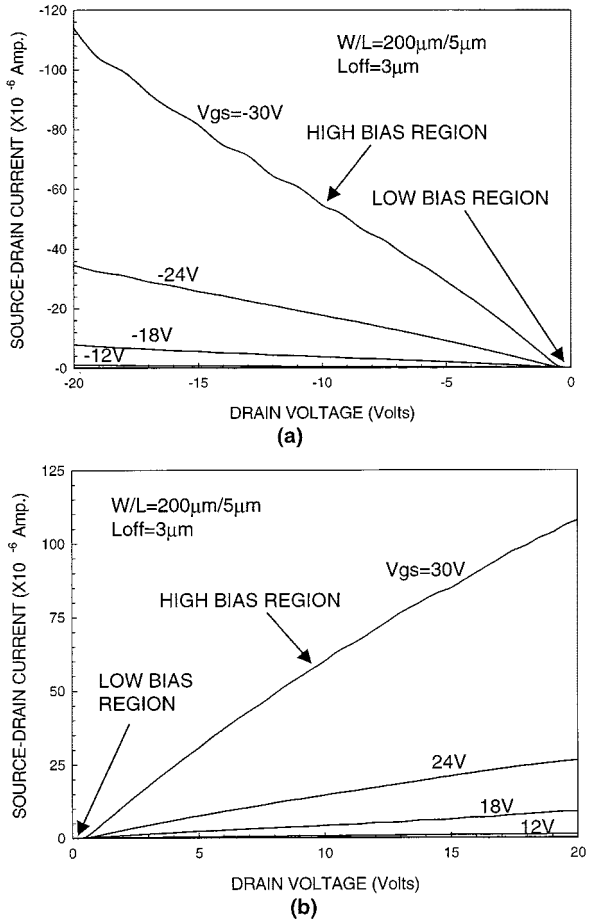

Fig. 3. *I–V* characteristics of the (a) p-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT, and (b) n-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT.

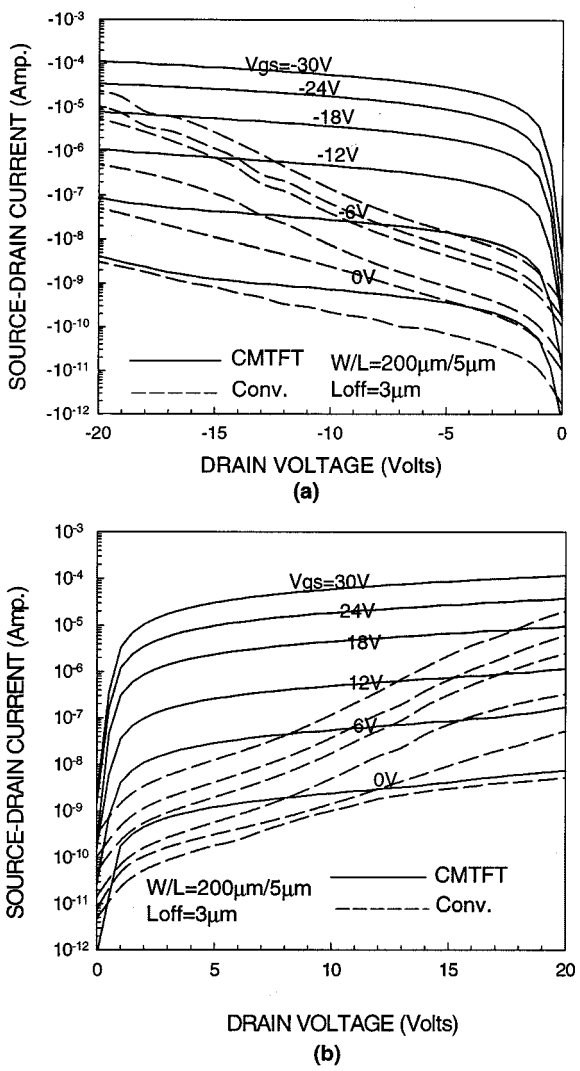

Fig. 4. Forward conduction characteristics of the (a) p- channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT and conventional offset drain TFT, and (b) n-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT and conventional offset drain TFT.

Å of LTO was deposited and densified at 600 °C for 12 h. The dopants were activated during the LTO densification. Contact holes were opened using dry etching of the LTO layer. A layer of Al was then deposited using the sputtering method with a target thickness of 1 μm. After metal patterning, forming gas annealing was performed at 350 °C for 30 min. Finally, the devices were hydrogenated in r.f. hydrogen plasma for 2 h.

IV. Results and Discussion

Fig. 3 shows the typical experimental *I–V* characteristics of both the p- and n-channel sandwiched CMTFTs. The *I–V* characteristics of both devices exhibit a low bias region and a high bias region. A transition voltage between the two regions is observed, which is in fact the turn-on voltage of the drain-diode. The transition voltage for the p- and n-channel devices are approximately -0.5 V and 0.5 V, respectively. At a drain voltage less than the turn-on voltage, the drain diode is off, and the device is basically off. As the drain voltage is increased beyond the diode turn-on voltage, the drain diode is turned on, and the device is operated in the high bias region. In this region of operation, minority carriers are injected into the offset region and modulate the offset region resistance for a significant increase in drain current.

Fig. 4 shows the forward conduction characteristics of the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched conventional offset drain TFT's and CMTFTs. All devices have the same offset length of 3 μm and W/L ratio of 200 μm/5 μm. It is shown that the on-state current of the p-channel CMTFT is 1.3 to 3 orders of magnitude higher than that of the conventional offset drain TFT at a gate voltage of -24 V and drain voltages ranging from -15 V to -5 V. While for the n-channel counterpart, 1.3 to 3.2 orders of magnitude higher on-state current is achieved at a gate voltage of 24 V and drain voltages ranging from 15 V to 5 V. The low on-state current of the p-channel (and n-channel) conventional offset drain TFT is due to the high resistance in the lightly doped offset region. When the drain voltage is low, most of the voltage is dropped across the offset region and the holes (electrons for the n-channel offset drain TFT) from the channel fill the traps at the grain boundaries in the offset region, resulting in a small drain current. Therefore, a higher drain voltage is needed to overcome the potential barrier caused by the grain boundary for higher drain current. In

the case of the p-channel (and n-channel) CMTFT (also shown in Fig. 4), a significantly higher on-state current is achieved, and the current pinching problem is minimized. This can be explained as follows. As the gate voltage is above the threshold voltage and the drain voltage is below the turn-on voltage of the drain diode, the drain diode is off and no electrons (holes for the n-channel) are injected from the drain. The device is off. When the drain voltage is increased beyond the turn-on voltage, the drain diode is turned on, electrons (holes for the n-channel) are injected into the offset region and lower the barrier height formed between the grain boundaries in the offset region. Such a reduction in the barrier height enhances the flow of both the holes and electrons. Thus, the conductivity in the offset region is modulated, and the on-state resistance is reduced dramatically. Hence, the on-state current is much increased.The threshold voltage and drive current capability of both the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched CMTFTs are listed in Table I. The poly-Si CMTFTs [10], [11] are also included for comparison. The threshold voltage of the p-channel devices is measured at a drain current of $-100\times$ (W/L) nA ($100\times$ (W/L) nA for the n-channel devices). Results show that both the p- and n-channel sandwiched CMTFTs have a higher threshold voltage than those of the poly-Si CMTFTs, indicating a higher trap density in the poly-$Si_{1-x}Ge_x$ film [5]. Since the threshold voltage is also a function of the current level (as defined above), the on-resistance in the offset region which determines the current level will also affect the threshold voltage. For the sandwiched CMTFTs, the n-channel device has a lower threshold voltage. This is due to the higher minority carrier (hole) mobility in the n-channel device compared to that of the minority carrier (electron) mobility in the p-channel device. The higher minority carrier mobility will make the resistance in the offset region lower, and in turn reduces the threshold voltage. In the case of the poly-Si CMTFTs, the n- channel device has a higher threshold voltage, which is also due to the lower minority carrier (hole) mobility in the poly-Si film.

Fig. 5 shows the gate transfer characteristics of the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched CMTFT and the conventional offset drain TFT before and after hydrogenation. The devices have the same dimensions as in Fig. 4. The threshold voltage, subthreshold slope, and leakage current are all improved after hydrogenation for both devices. The leakage currents of the CMTFTs are comparable with those of the conventional offset drain TFT's. The p-channel (and n-channel) CMTFT has a six times (five times[1]) higher on/off current ratio than that of the conventional offset drain TFT at a drain voltage of -20 V (20 V*) and a gate voltage of -24 V (24 V*).

To compare the drive current capability of the various devices, the on-current (measured at V_{gs} =30 V and V_{ds} =20 V for the n-channel, $V_{gs} = -30$ V and $V_{ds} = -20$ V for the p-channel) normalized to the threshold voltage of the devices $(V_{gs}–V_{th})$ is obtained. It can be seen that the p-channel sandwiched CMTFT has a 60% higher current drive capability than that of the poly-Si CMTFT, which is due to the higher hole mobility in the poly-$Si_{1-x}Ge_x$ film. However, for the n-channel devices, the poly-Si CMTFT has a 3.3 times higher drive current capability than that of the sandwiched n-channel CMTFT. This is due to the lower trap density in the poly-Si film, which has

[1]Values within the parentheses are for the n-channel devices.

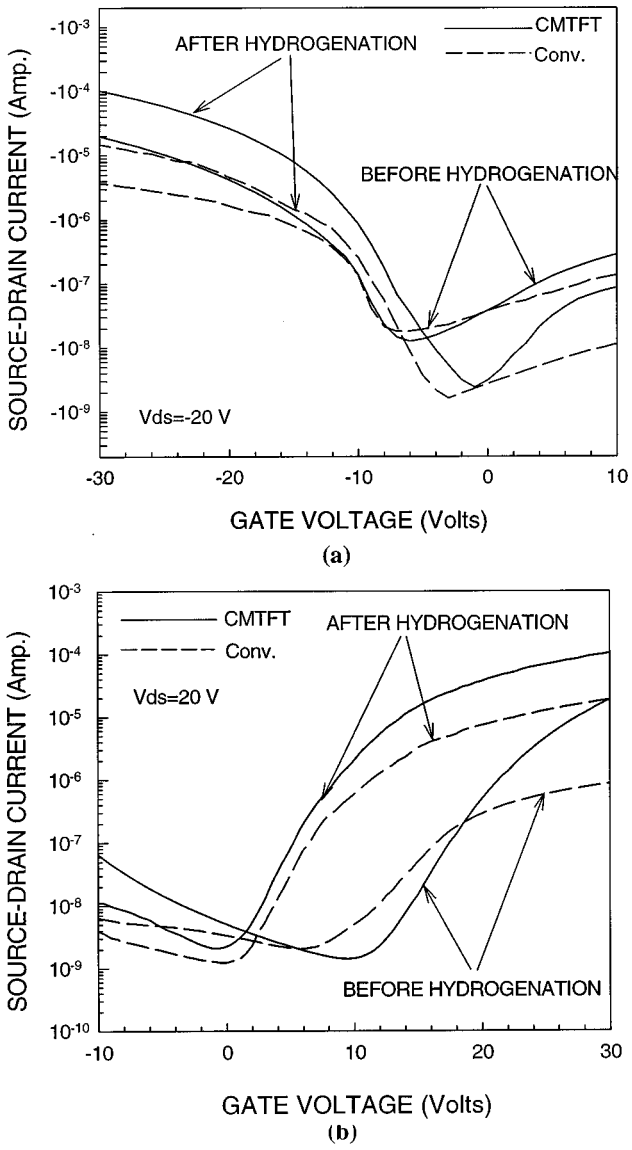

Fig. 5. Gate transfer characteristics of the (a) p-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT and conventional offset drain TFT, and (b) n-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT and conventional offset drain TFT.

TABLE I
COMPARISON OF BOTH THE P- AND N-CHANNEL POLY-Si/$Si_{1-x}Ge_x$/Si CMTFT'S WITH THE POLY-Si CMTFTs [10], [11]

Parameters	Poly-Si/$Si_{1-x}Ge_x$/Si CMTFT		Poly-Si CMTFT	
	n-channel	p-channel	n-channel	p-channel
V_{th} (V)	11.5	-13	10	-8
$I_{on}/(V_{gs}-V_{th})$ (μA/V)	5.4	7.0	18.0	4.4

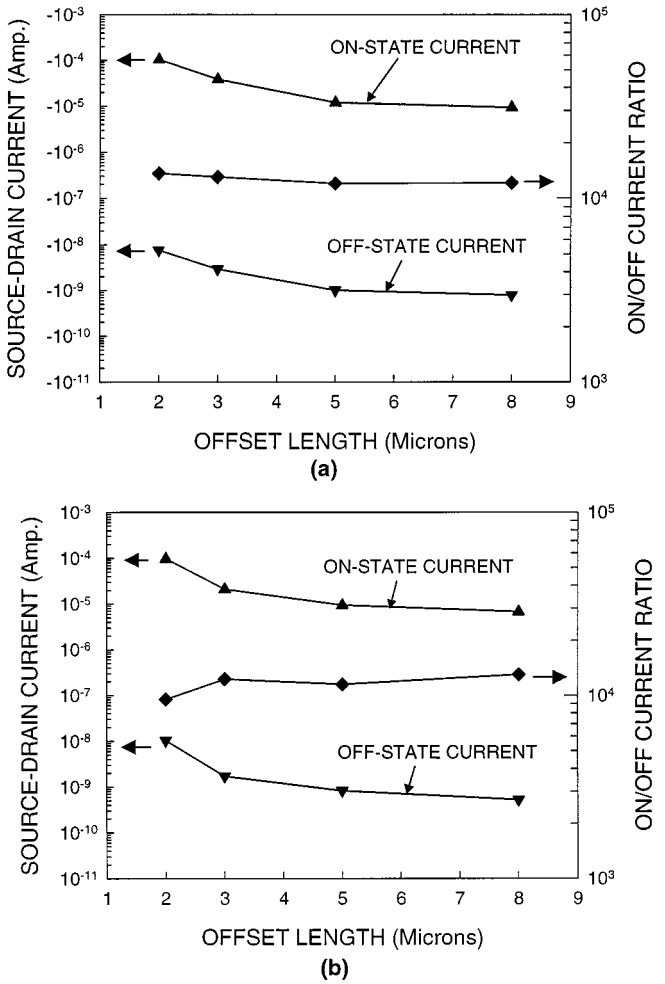

Fig. 6. On-state and off-state current versus offset length of the (a) p-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT and (b) n-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT.

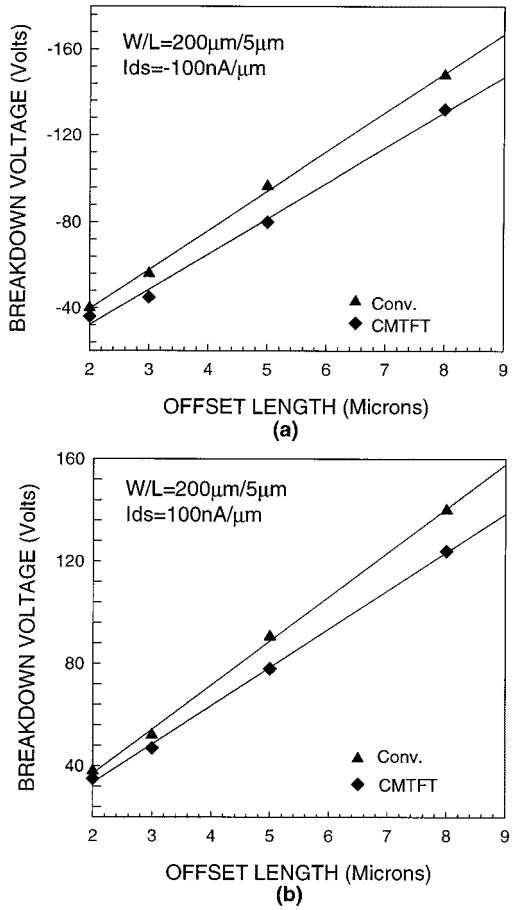

Fig. 7. Breakdown voltage versus offset length of the (a) p-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT and (b) n-channel poly-Si/$Si_{1-x}Ge_x$/Si CMTFT.

a lower on-state resistance in the offset region. To improve the performance of both the p- and n-channel poly-SiGe CMTFT's, higher quality poly-SiGe film obtained using laser recrystallization or lateral recrystallization will be needed.

The on-state and off-state currents of the p-channel (and the n-channel) CMTFTs as a function of the offset length are shown in Fig. 6 with W/L of 200 μm/5 μm. The on-state current is measured at a drain voltage of -20 V (20 V*) and a gate voltage of -24 V (24 V*). As expected, the on-state current of the devices decreases with an increase in the offset length[2]. As the offset length increases, the on-state resistance increases, which leads to a reduction on the on-state current of the devices. The off-state current is measured at a drain voltage of -20 V (20 V*) and a zero gate voltage. The off-state current also decreases with an increase in the offset length. As the offset length increases, the lateral electric field at the drain region decreases, resulting in a corresponding reduction on the off-state current. Since both the on-state and off-state currents are reduced at a longer offset length, a relatively constant on/off current ratio is obtained. The on/off current ratio as a function of the offset length is also shown in Fig. 6.

Fig. 7 shows the breakdown voltage of the p- and n-channel CMTFTs as a function of the offset length. The devices are with a W/L ratio of 200 μm/5 μm. The breakdown voltage of the p- and n-channel devices is measured at a drain current of -100 nA/μm and 100 nA/μm, respectively. It is shown that the breakdown voltage increases fairly linearly with an increase of the offset length. This is due to a reduction of electric field at the drain junction as the offset length is increased, which lowers the impact ionization and in turn causes the breakdown to occur at a higher voltage. The breakdown voltages of the p- and n-channel conventional offset drain TFTs as a function of the offset length are also shown in Fig. 7 for comparison. For the p-channel (and the n-channel) CMTFT, the large drain voltage is supported by a parallel combination of a $p^+/i/n^+$ ($n^+/i/p^+$ for the n-channel) diode structure and an n^+-segmented/i/n^+ (p^+- segmented/i/p^+ for the n-channel) resistor structure. However, in the case of the p-channel (and the n-channel) conventional offset drain TFT, the breakdown voltage is determined by a $p^+/i/p^-/p^+$ ($n^+/i/n^-/n^+$ for the n-channel) resistor structure. The results, shown in Figs. 6 and 7, also demonstrate that a high breakdown voltage p- and n-channel CMTFT with a high on/off current ratio can be obtained.

[2]There is a discrepancy (~10%) in the current values compared with those in Fig. 4. The discrepancy is mainly due to the offset rehion variation which arises form the nisalignment when doping the drain region. Non-uniformity of the grain size in the poly-SiGe film also causes the current to be different.

Although both the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched CMTFTs have involved minority carriers (electrons for the p-channel and holes for the n-channel) in the conduction mechanism, no degradation in the switching speed of the devices was observed. This agrees with the switching performance of the poly-Si CMTFTs reported earlier [10], [11]. In fact, the lifetimes for the minority carriers in the poly-$Si_{1-x}Ge_x$ material are even shorter compared to those in the poly-Si material. This is expected since the poly-$Si_{1-x}Ge_x$ has a higher trap-state density than that in the poly-Si material [5].

V. Conclusion

Both the p- and n-channel poly-Si/$Si_{1-x}Ge_x$/Si sandwiched CMTFTs were demonstrated and analyzed. The conductivity modulation effect observed in the poly-$Si_{1-x}Ge_x$ material is as effective as that in the poly-Si material. Results show that the transistors provide a high on- state current as well as a low leakage current compared to those of the conventional offset drain structures. CMOS CMTFTs fabricated on the poly-$Si_{1-x}Ge_x$ material can be designed for use in low temperature large area electronic applications.

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