Characterization and minimization of flicker in silicon light valves

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We have performed systematic characterizations of flicker in silicon light valves. It was found that there were four conduction mechanisms accounting for the flicker. These four mechanisms were residual dc charge on the silicon surface, voltage holding capability of the liquid crystal cell, voltage holding capability of the silicon panel, and parasitic capacitor coupling of the pixel. Major causes of these four mechanisms were identified. Solutions of flicker minimization were obtained for each mechanism. Among these solutions, offset of common voltage was found very useful to compensate for residual dc charge and parasitic capacitor coupling. Frame rate multiplication was found very useful for the minimization of flicker due to low voltage holding capabilities of the liquid crystal cell and silicon panel. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1331073]

I. INTRODUCTION

Flicker is a major visual defect in active matrix liquid crystal displays (AMLCDs). As the AMLCD becomes more popular, there have been increased research activities on flicker in order to minimize this undesirable effect.[1–5] However, most of these studies were focused individually on LC mixtures[1,2] or alignment layers.[3] For example, Jacob *et al.* of Merck investigated specific resistivity and capacitance of LC mixtures, and suggested a minimal specific resistivity of $5\times10^{12}\ \Omega$ cm to ensure the voltage holding capability of a LC cell.[1] Sato *et al.* of Nissan Chemical studied various kinds of alignment layers for their charge accumulation potentials, and obtained new alignment film materials to reduce extra charge accumulation.[3] There were also a few studies on pixel structures and driving methods for the minimization of flicker. Kodate *et al.* of IBM reported photoinduced flicker on high-resolution AMLCD, and proposed a low reflectance black matrix on pixel transistors to reduce visual cross talk.[4] Nishimura *et al.* of Mitsubishi used multidot inversion and dual gate selection to minimize flicker for a UXGA AMLCD.[5] But so far, there was no systematic approach to identify causes of flicker and to minimize flicker accordingly in the AMLCD.

The AMLCD depends on active devices to apply voltages onto the pixels during address time and the ability of pixels to conserve the voltage for the rest of the frame time. To avoid chemical degradation of the LC material, an alternating voltage wave form has to be applied to the LC cell. For this purpose, several modes of polarity inversion including frame, column, row, and dot inversions are adopted. Each mode has its advantages and disadvantages. The frame inversion is commonly used in silicon light valves for the purpose of minimizing lateral electric field in small pixels.[6] The lateral electric field can result in an undesired reverse tilt domain in each pixel and lead to poor contrast of the display.[7] While the frame inversion is good for minimizing the lateral field effect, it also produces a higher degree of flicker compared with other modes of polarity inversion.

In this work, we performed systematic characterizations of flicker in silicon light valves and aimed at minimizing the flicker appropriately. New pixel structures, different alignment films, LC mixtures, reflective LC modes, and driving methods were evaluated. Four experiments were designed to probe conduction mechanisms within silicon light valves for causes of flicker. Through the systematic characterizations of flicker in various silicon light valves, a flicker model was established. Solutions of minimizing this visual defect were obtained to improve the silicon AMLCD quality.

II. ORIGINS OF FLICKER

Flicker can be characterized by monitoring luminance of the same image on the display in alternative frames. A larger luminance difference corresponds to a higher degree of flicker. We defined the flicker as a ratio of ac root-mean-squared luminance over dc root-mean-squared luminance. Since the luminance is controlled by pixel voltage, the flicker can also be characterized through monitoring of the pixel voltage. The voltage retention capability of the pixel is described by an equivalent circuit consisting of a storage capacitor connected to a substrate ground and a LC cell capacitor with a parallel leakage resistance connected to a common electrode on the glass plate.

The voltage holding ratio (VHR) is defined as the ratio of root-mean-squared voltage divided by the applied voltage pulse on a pixel electrode. The value is mainly determined by RC time constant of the LC pixel and auxiliary storage capacitor. The RC time constant can be calculated from the resistivity and dielectric constant of the LC material and the geometry of the pixel. There are two causes for the decrease of VHR on the silicon panel. One is leakage current through the *n*-type pixel transistor to *p*-type substrate. This leakage can be represented by a saturation current of a reverse-biased

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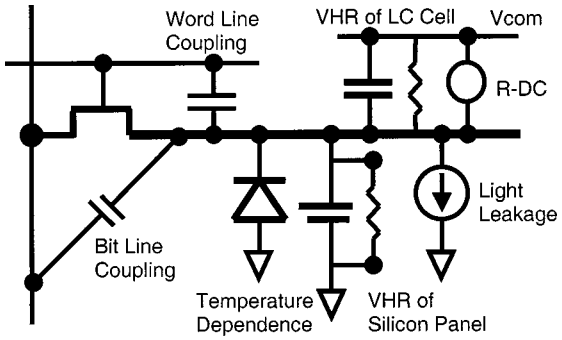

FIG. 1. Flicker model of the pixel.

$p-n$ junction diode. The other is photocurrent generated by light leakage onto the silicon substrate. This leakage can be modeled as a current source of a photodiode in photoconductive mode. In addition, there are different conduction mechanisms in polar liquids in combination with other dielectric layers in the AMLCD. The conduction mechanism can perturb charge distribution within the LC element and enhance the flicker. This conduction mechanism can be represented by a residual dc (Rdc) charge on the pixel.

In addition to the LC cell and pixel transistor, word and bit-line voltages in the active matrix can also contribute to the flicker. The word line turns on the pixel transistor for charging. But the pixel voltage is pulled down slightly through a parasitic capacitor coupling when the pixel transistor is turned off by word line. The bit-line voltage varies randomly and perturbs the pixel voltage randomly. But the perturbation becomes coherent when the polarity of inversion is changed. As a result, the pixel voltage is pushed up or pulled down through the bit-line and pixel capacitor coupling. These two kinds of capacitor couplings can be represented by two parasitic capacitors connected from the pixel to the word and bit lines, respectively. A flicker model of the pixel is illustrated in Fig. 1.

III. SILICON LIGHT VALVE SAMPLES

In our earlier work, we developed a highly integrated liquid crystal-on-silicon light valve for a three-panel color projector.[8] The silicon panel was designed and fabricated by a custom 0.5 μm and three-metal complimentary metal–oxide–semiconductor technology with a XGA resolution of 1024×768 pixels. The pixel pitch was 13.8 μm and the fill factor was 91%. A mixed twisted nematic and birefringence (MTB) cell configuration was employed onto the panel.

The silicon light valve samples were prepared for the purpose of flicker characterizations. New pixel structures were proposed. The ratio of storage over parasitic capacitor was varied for different degrees of charge deviation. A larger capacitor ratio could minimize the charge deviation and a larger storage capacitance could better preserve the pixel voltage. Charge deviation on the flicker could be quantified. Within the pixel structure, a low reflectance black matrix was inserted for light leakage protection. On the pixel surface, different passivation layers were coated for protection of the pixels. These passivation layers included bare metal, thin oxide, oxide/nitride, multilayer oxide/nitride, and dielectric mirror. Different passivation layers had different work functions and could trap ions by interfacial states. Ions trapped on the flicker were measured for different passivation schemes.

In addition to pixel structures and passivation, different alignment films of different thickness were coated onto the silicon panel. The alignment layer was required and used to align the LC mixtures in particular directions for particular LC mode operation. The alignment layer might trap a charge and cause a flicker. Charge trapped on the flicker could be quantified for different alignment films of different thickness. Finally, LC mixtures of high specific resistivity and capacitance were used to make MTB LC cells on top of silicon panels. The LC mixture was the most important optical component for silicon light valves. Its voltage holding capability and temperature stability greatly affected the flicker. Both the LC cells and silicon light valves of the same cell configuration were prepared for different kinds of characterizations.

IV. FLICKER CHARACTERIZATIONS

Four experiments were designed to probe conduction mechanisms within the silicon light valve samples. The first one was a capacitance–voltage ($C-V$) measurement of the LC cell in order to determine cell capacitance and parallel leakage resistance. Through this characterization, the LC cell was modeled as an equivalent circuit of a parallel capacitor and resistor. The second one was an Rdc measurement of the LC cell in order to determine extra charge accumulation on surface of the LC cell. The LC cell was illuminated by different light intensities at evaluated temperature. A square wave was applied to the cell and a photodetector in connection with a digital oscilloscope and was used to monitor reflectance of the cell. Flicker was recorded and a dc offset voltage was in 10 mV steps until the flicker was no longer observed. This dc offset voltage was denoted as an Rdc voltage.

The third one was a VHR measurement of the pixel made by the LC cell, a pixel transistor, and a storage capacitor. A short pulse of voltage was applied to the pixel during address time and charge was preserved by the pixel during the rest of the frame time. The pixel voltage was buffered and amplified by a high-impedance operational amplifier and monitored by a digital oscilloscope. Voltage holding capability of the pixel at different temperatures was recorded. The VHR characterization could be performed simultaneously with the Rdc measurement.

The last one was a direct measurement of flicker on the pixel array of a silicon light valve. A video pattern generator was used to drive the silicon light valve at different frame rates and in different polarities of inversion. A photodetector, in connection with a digital oscilloscope, was used to monitor luminance of the projected image. Flicker was recorded and a dc offset voltage was increased on the common electrode until the flicker was minimized. A more detailed flicker mechanism could be observed from this characterization.

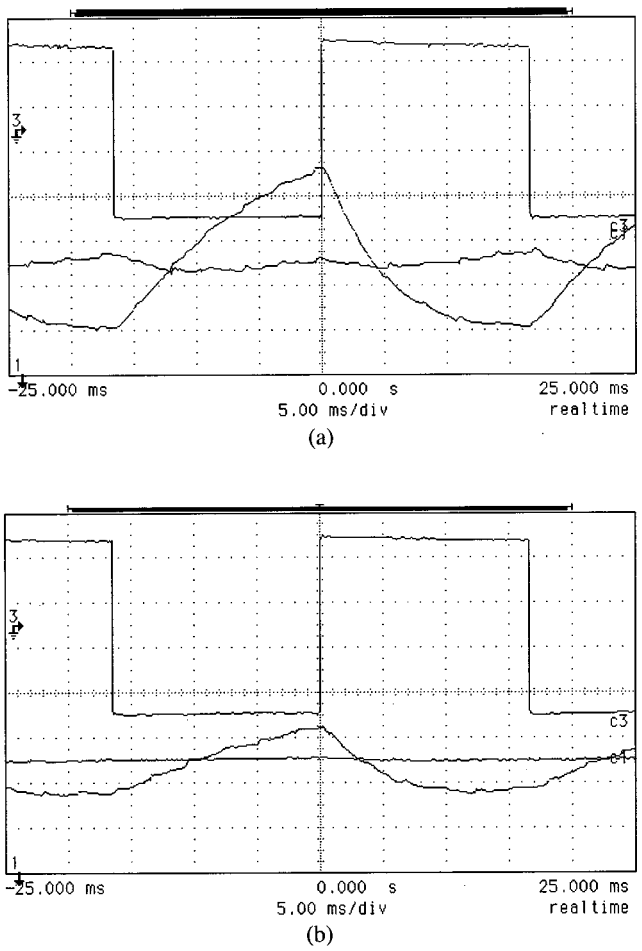

FIG. 2. Rdc and VHR measurement results of two LC cells of (a) multilayer passivation and (b) no passivation.

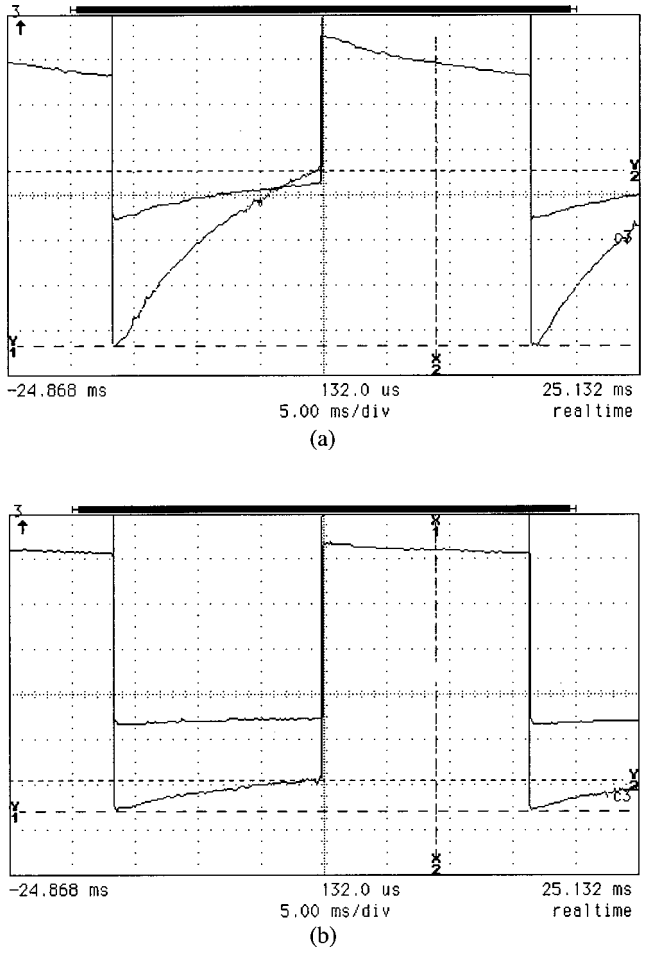

FIG. 3. VHR measurement results of two LC cells of (a) 5×10^{11} and (b) 5×10^{12} Ω cm specific resistivity.

V. CHARACTERIZATION RESULTS

Figure 2 shows Rdc and VHR measurement results of two LC cells of different passivation. The upper trace was the pixel voltage holding curve observed by the VHR measurements. Both the curves in Fig. 2(a) and 2(b) decayed 3% at a 60 Hz frame time and corresponded to a VHR of 97% for the LC cell. The lower two traces denoted luminance of the display under a 150 W lamp. The incident light intensity on the LC cell was 2×10^6 lumen/m^2 (or lux). One trace had no common voltage (Vcom) compensation and exhibited flicker. The other had Vcom compensation and exhibited minimal or no flicker. The cell with multilayer passivation had a flicker ratio of 42%, which could be reduced to 5% by a Vcom offset voltage of 200 mV. The other cell with bare metal or no passivation had a flicker of 15%, which could be reduced to 0% by a Vcom offset voltage of 50 mV. The LC mixtures used in both cells had a specific resistivity of 5×10^{12} Ω cm as suggested by Jacob *et al.* of Merck.[1] As a result, the VHR of the LC cell was high and contributed no flicker.

Figure 3 shows the VHR measurement results of two LC cells of different LC mixtures, which had specific resistivity of 5×10^{11} and 5×10^{12} Ω cm, respectively. The VHR curves in Fig. 3(a) decayed by an ac root-mean-squared voltage of 380 mV from 2 V and corresponded to a VHR of 81% for the LC cell of low resistivity. The VHR curves in Fig. 3(b) decayed by 60 mV and corresponded to a VHR of 97% for the LC cell of high resistivity. The flicker ratios were 30% and 6%, respectively, without Rdc compensation. Both LC cells had the same oxide/nitride passivation and were driven by a 2 V square wave of a 60 Hz frame rate.

Figure 4 shows flicker measurement results of a typical

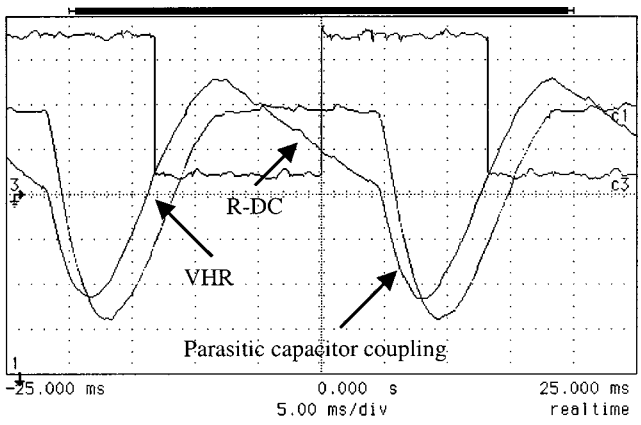

FIG. 4. Flicker measurement results of XGA silicon light valve.

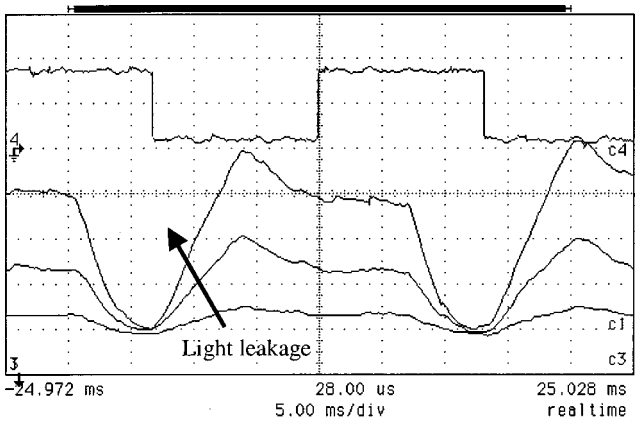

FIG. 5. Flicker measurement results of XGA silicon light valve under different light illuminations.

silicon light valve. There were three flicker mechanisms observed in the lower two luminance curves. One was a hot-state Rdc voltage caused by the passivation layer. The second was insufficient VHR of the silicon panel. The pixel voltage was decayed and exhibited an increase of optical reflectance in a normally white (NW) light valve. The third was bit-line coupling, which occurred when the polarity of frame inversion was reversed. The pixel voltage was pushed up and exhibited a decrease of optical reflectance in a NW light valve. The polarity of frame inversion was denoted by the upper trace. Figure 4 also shows compensation of the hot-state Rdc charge by a Vcom offset voltage of 200 mV. The luminance curve was flattened in that region, but the flicker was not reduced too much because the hot-state Rdc charge was not the principal flicker mechanism in this characterization.

The principal flicker mechanism in this characterization was the VHR of the silicon panel. The pixel voltage could not be held during the frame time, but was decayed through leakage. It was found that both temperature and light leakage could contribute to this insufficient VHR of the silicon panel. Whereas, the temperature exponentially increased the saturation current of the pixel transistor. While the light leakage drained pixel charge from the storage capacitor. The VHR of the panel was improved as the light intensity was reduced from 2×10^6 to 1.4×10^6 and 7×10^5 lux as shown in Fig. 5.

Figure 6 shows flicker measurement results of two silicon light valves of different cell configurations. One light valve was made of NW MTB mode,[9] which had a twisted angle of 70°, a polarizer angle of 30°, and a retardation of 0.31 μm. The other was made of normally black (NB) MTB mode, which had a twisted angle of 52°, a polarizer angle of 0°, and a retardation of 0.53 μm. It was found that the NW mode had a lesser degree of flicker as shown in Figure 6(a). The measured ac and dc root-mean-squared (rms) luminance were 0.138 and 3.48 V, respectively, and corresponded to a 4% flicker ratio. The NB mode exhibited a larger degree of flicker as shown in Fig. 6(b). The measured ac and dc root-mean-squared luminance were 0.21 and 2.98 V, respectively, and corresponded to a 7% flicker ratio.

The LC cell is to convert an electronic signal into an optical signal through electro-optical modulation. Each LC

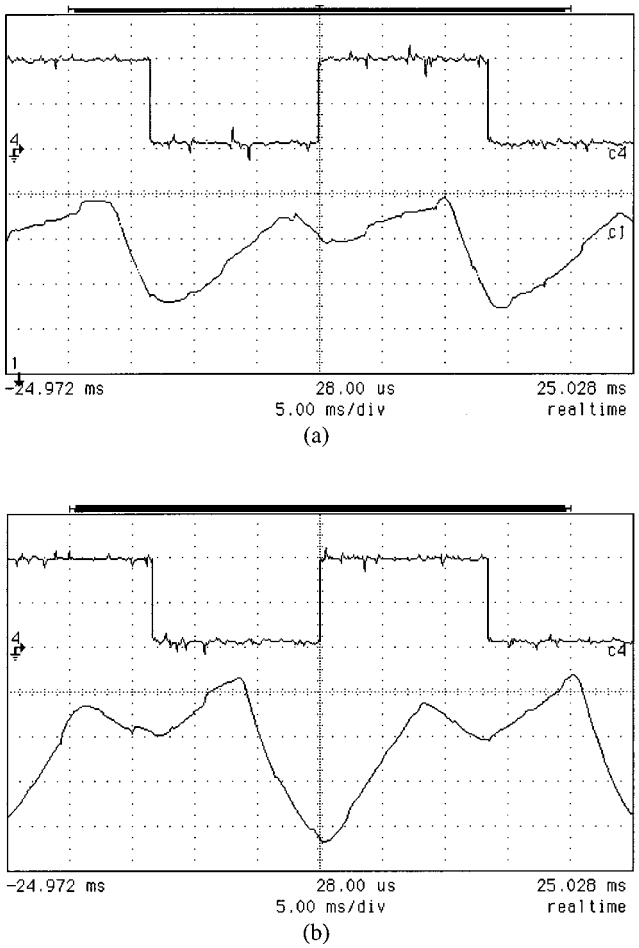

FIG. 6. Flicker measurement results of two different silicon light valves of (a) NW and (b) NB modes.

mode has its own reflectance versus voltage characteristic. Figure 7 shows measured reflectance versus voltage curves of these two silicon light valves of NW and NB modes, respectively. It was observed that the NW mode had a wider modulation voltage range from 1.3 to 3.3 V, and the NB mode had a narrower modulation voltage range from 1.1 to 2.1 V. While the NB mode had the advantage of low voltage operation, it also showed high reflectance vs voltage sensi-

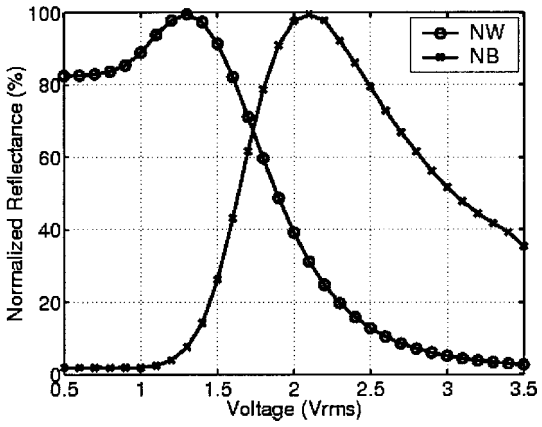

FIG. 7. Reflectance vs voltage curves of NW and NB modes.

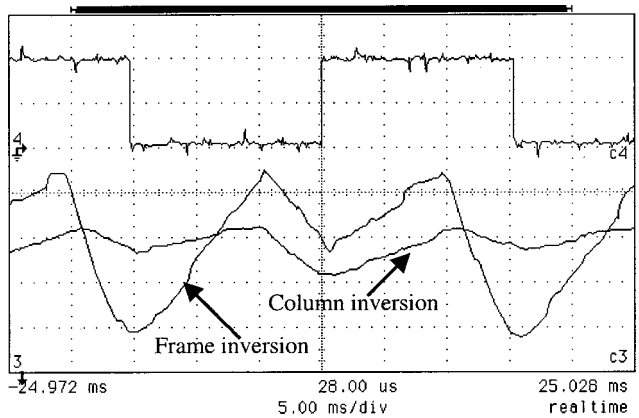

FIG. 8. Flicker measurement results of the same XGA silicon light valve under frame and column inversions.

tivity. The reflectance versus voltage sensitivity was 0.18%/mV at 50% reflectance point for the NB mode. In comparison, the sensitivity was only 0.1% for the NW mode. Because of this sensitivity difference, the NB mode exhibited a larger degree of flicker.

Figure 8 shows flicker measurement results of the same silicon light valve under frame and column inversions. The column inversion could average the flicker spatially in alternative columns. As a result, the column inversion produced a lesser degree of flicker than that of the frame inversion. Figure 8 also shows perturbation of the parasitic capacitor coupling to the flicker when the polarity of inversion is changed. In the positive polarity of frame, the bit lines carried positive voltage with respect to the common voltage on the glass plate, and charged the pixels to positive voltages. When the polarity of frame was changed from positive to negative, the positive pixel voltages (previously charged in the positive polarity of frame) were pulled down by the parasitic capacitor coupling. As a result, the root-mean-squared pixel voltage was reduced and hence, the reflectance was increased right after the change of frame polarity for the NW mode. However, this perturbation was not observed in the column inversion because of spatial average of perturbation and flicker.

Finally, Figure 9 shows flicker measurement results of a silicon light valve at elevated temperature from 20 to 60 °C. The flicker was 6% and remained about the same at temperatures below 30°C. Different conduction mechanisms contributed to the flicker and there was apparently not a dominated one from the luminance curves of 20 and 30 °C in Fig. 9. As the temperature was increased beyond 40 °C, the luminance curves showed characteristics of insufficient VHR of the silicon panel. The pixel voltage in the negative polarity of frame was discharged toward the substrate ground and decayed away from Vcom. As a result, the luminance was decreased for the NW light valve. In the positive frame of polarity, the pixel voltage was discharged toward the substrate and Vcom. As a result, the luminance was increased for the NW light valve. The flicker was increased from 8% at 40 °C, to 15% at 50 °C, and to 22% at 60 °C.

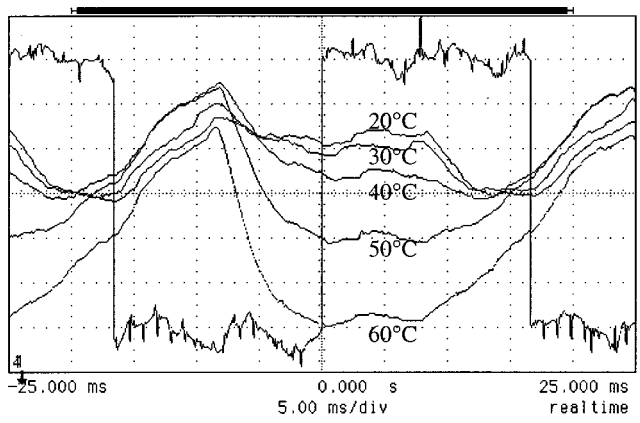

FIG. 9. Flicker measurement results of XGA silicon light valve at elevated temperature from 20 to 60 °C.

VI. SOLUTIONS OF FLICKER MINIMIZATION

Through these flicker characterizations, we have identified causes of flicker for each mechanism. We proceeded to find out solutions of flicker minimization for each mechanism. The Rdc charge accumulation was mainly caused by different work functions of the indium–tin–oxide (ITO) glass plate and silicon surface. Different passivation schemes had different interfacial states with LC layer and could perturb the Rdc charge as well. The Rdc charge per unit area can be expressed as

$$Q_{\mathrm{Rdc}} = q(\phi_{\mathrm{Al}} - \chi_{\mathrm{ITO}}) + q(D_{\mathrm{Si}} - D_{\mathrm{ITO}}). \quad (1)$$

Where ϕ_{Al} is the work function of aluminum, the pixel electrode; χ_{ITO} is the electron affinity of ITO; D_{ITO} and D_{Si} are interfacial charge density states of the ITO and silicon surface, respectively. The work function of aluminum is 4.3 eV and the electron affinity of a heavily doped *n*-type ITO is 4.1 eV.[10] As a result, the work function difference between these two asymmetrical electrodes was only 0.2 eV and did not contribute much to the Rdc charge. This was revealed in our characterization that the measured Rdc voltages were always less than 50 mV, and typically 30 mV for those LC cells and light valves with no passivation on the pixel electrode.

The surface charge density states on the silicon surface could trap a Rdc charge. From the Rdc measurements, we found that the multilayer passivation had more interfacial states to trap extra charge on the silicon surface. The measured Rdc voltages were larger than 200 mV and typically 300 mV for those LC cells and light valves with oxide/nitride/oxide/nitride passivation on the pixel electrode. In comparison, oxide or oxide/nitride passivation had less interfacial states for extra charge accumulation. The measured Rdc voltages were between 30 and 150 mV, and typically 90 mV, for these LC cells and light valves with oxide or oxide/nitride passivation.

The measured Rdc voltages for all four passivation schemes had a normalized standard deviation of about 30%. We believed this deviation was due to the contamination introduced during the LC cell assembly. The contamination might perturb the interfacial charge density states on both the ITO and silicon surface. As a result, the Rdc voltage of the same kind of passivation was moderately changed. The Rdc

charge was not a big concern for flicker in silicon light valves and could be reduced efficiently by Vcom compensation on the glass plate.

We have also applied different alignment film materials in silicon light valves, and varied the thickness from 200 to 1000 Å. The alignment film has more direct contact with LC mixtures and would probably affect the Rdc charge on the surface of LC cell. But we did not observe a significant difference in terms of Rdc charge for those LC cells with different film parameters. It was concluded that the film was too thin and its contribution to the charge accumulation on the silicon surface of the LC cell was insignificant.

The VHR of a LC cell was mainly determined by specific resistivity of the LC mixture. Different passivation schemes or alignment films did not affect the VHR of the LC cell too much. A higher specific resistivity could give rise to a higher leakage resistance and hence a lower VHR of the LC cell. It was found that the specific resistivity of LC mixture had to be larger than 5×10^{12} Ω cm in order to achieve more than 97% VHR of the LC cell at a 60 Hz frame rate. An even higher VHR could be achieved with a LC mixture of higher specific resistivity or at a higher frame rate. But, 97% VHR was considered adequate in terms of flicker minimization. The 97% VHR corresponded to 60 mV voltage deviation at 2 V rms driving, which gave rise to most voltage sensitive 50% reflectance point. This 60 mV voltage drift could exhibit a 6% luminance difference for a typical NW mode of 0.1%/mV reflectance versus voltage sensitivity, if the LC cell responded immediately to the voltage. But the LC cell would not respond immediately to the voltage change within the 60 Hz frame time. As a result, this small voltage deviation in the same frame would not contribute too much to the flicker and could be totally compensated by several means.

The VHR of silicon panel was determined mainly by temperature and light leakage. Whereas the temperature increased exponentially, saturation current of the pixel transistor and light leakage generated photocurrent and drained the pixel charge out of the storage capacitor. We modeled the temperature effect by a saturation current of a reverse-biased $p-n$ junction diode. The saturation current has significant temperature dependence and can be expressed as[11]

$$I_S(T)=I_{S0}T^{XTI}\exp\left(-\frac{E_g(T)}{kT/q}\right), \tag{2}$$

where I_{S0} is the saturation current constant and independent of temperature; XTI is the empirical temperature coefficient and its value is 3 for the silicon diode; k is the Boltzmann constant; T is temperature in °K; q is the elementary charge, and $E_g(T)$ is the energy band gap, which also has strong temperature dependence and can be expressed in an empirical form as

$$E_g(T)=E_{g0}-GAP1\cdot\frac{T^2}{T+GAP2}, \tag{3}$$

where E_{g0} is 1.16 eV, $GAP1$ and $GAP2$ are 7.02×10^{-4} eV/°K and 1108 °K for silicon, respectively. The leakage current at room temperature of 25 °C was about 0.3 pA, which was calculated from the dimensions of the pixel transistor and wafer manufacturer's data. But this current was increased abruptly to 3.5 pA at 40 °C, 15 pA at 50 °C, and 60 pA at 60 °C according to Eqs. (2) and (3). The voltage deviation due to the leakage current at a time interval of Δt can be expressed in the following way:

$$\Delta V=\frac{I_S\cdot\Delta t}{C_{\mathrm{LC}}}+C_S, \tag{4}$$

where C_{LC} and C_S are capacitance of LC cell and storage capacitors, respectively. In our silicon light valve samples, the storage capacitance had a larger valve than the LC cell capacitance. The total value was about 0.4 pF. For a 60 Hz frame time of 16.7 ms, the voltage deviation due to the leakage current of 0.3 pA at 25 °C was only 12 mV. This value was smaller than those values due to Rdc charge, VHR of the LC cell, and parasitic capacitor coupling. But as the leakage current was increased with temperature, the voltage deviation was also increased to 140 mV, 600 mV, and 2.4 V at 40, 50, and 60 °C, respectively. The leakage of the pixel transistor became the dominant flicker mechanism when the temperature was beyond 40 °C.

Temperature is the most important cause of flicker. High temperature could reduce VHR of the silicon panel through leakage current of the pixel transistor. High temperature could also reduce VHR of the LC cell through leakage current in the LC mixture. As a result, temperature was reduced to 25 °C or below through passive heat sink in all of our other flicker characterizations. Once this primary cause of flicker was removed, other secondary causes of flicker could be observed through the characterizations. For the VHR of the silicon panel, the secondary cause of flicker is light leakage. The light leakage onto the silicon substrate generates photocurrent, which is proportional to the light illuminance and can be expressed in the following way:

$$I_\lambda=\frac{\eta MAq}{h\nu}, \tag{5}$$

where η is effective conversion efficiency, M is light irradiance falling onto the pixel with a light leakage area A, $h\nu$ is photon energy at wavelength λ. In our silicon light valve samples, the pixel area was fully covered with a light shield by overlapping metal layers. There was no open area exposed directly to the incident light. However, light still could zigzag into the silicon substrate through two reflections at metal layers. The metal layers had antireflection coating on both sides and allowed for 10%–15% reflection. As a result, the penetrated light was attenuated to only 1%–2% through two reflections. Assuming a perfect conversion efficiency and 1 μm^2 light leakage area on pixel, the generated photocurrent was about 4 pA at 1×10^6 lux green light illumination according to Eq. (5). But the conversion efficiency was much less than 100% since the p-type substrate was not a good photodetector. A more practical estimation of the photocurrent was about 1 pA from Fig. 5, which also showed that the photocurrent increased proportionally with illuminance. Minimization of light leakage could be obtained through a pixel structure of better light shield protection. A larger storage capacitance could also help in minimizing the flicker due to the leakage current and photocurrent.

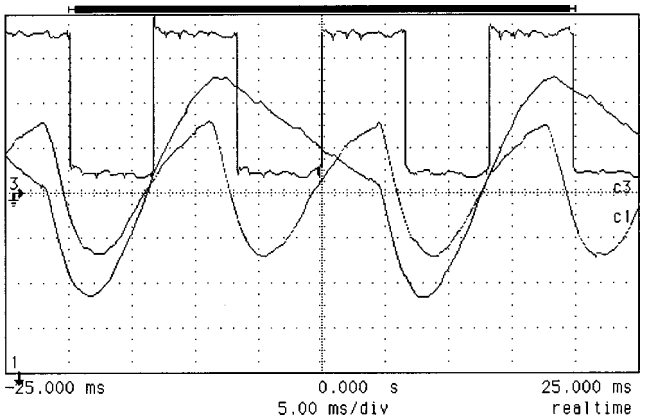

FIG. 10. Minimization of flicker by frame rate multiplication.

The parasitic capacitor coupling was determined by magnitudes of parasitic and storage capacitance. A larger ratio of the storage over parasitic capacitance could reduce the coupling. It was found that a minimal ratio of 80 was required to minimize the coupling. For a 2 V rms or 4 V peak-to-peak driving at 50% reflectance point, this 1/80 coupling ratio corresponds to 50 mV voltage deviation in alternative frames. However, a ratio of larger than 80 could not be achieved when the pixel was reduced to a 10 μm pitch. At this pitch, most of the pixel area was used for the pixel transistor, and not much was left for the storage capacitor. It was found that imbalance driving was useful to compensate for the charge deviation caused by the parasitic capacitor coupling. In this regard, the pixel voltage was charged higher in the positive polarity of the frame to allow for the loss in the positive-to-negative frame coupling. In contrast, the pixel voltage was charged lower in the negative polarity of the frame to allow for the gain in the negative-to-positive frame coupling. Offset of common voltage was also useful for the compensation of the parasitic capacitor coupling.

Reflective LC modes of different reflectance versus voltage sensitivity could also affect the flicker. For a same VHR of the LC cell and silicon panel, a LC mode of low reflectance versus voltage sensitivity was favored to exhibit a lower luminance difference or flicker. For this concern, the NW reflective LC mode operated with a polarizing beam splitter was preferred. The reflectance versus voltage sensitivity for a typical NW reflective LC mode was 0.1%/mV.

Finally, frame rate multiplication was found very useful to minimize the flicker. For example, double of the frame rate could reduce the flicker by about half as shown in Fig. 10. In this characterization, the VHR of the LC cell was reduced by half because the charge deviation due to LC leakage was only half in the half frame period. The VHR of the silicon panel was also reduced by half because the charge deviation due to light leakage was only half in the half frame period. Rdc charge on silicon surface could always be compensated by the offset of common voltage and contributed no flicker. Parasitic capacitance coupling could be compensated through imbalance voltage driving and contributed very little flicker. As a result, a simple frame rate multiplication reduced the flicker by half in this characterization.

VII. CONCLUSION

We have performed a systematic characterizations of flicker in silicon light valves. It was found that there were four mechanisms accounting for the flicker. The residual dc charge was caused by different work functions of the ITO glass plate and the silicon surface, and could be reduced through a suitable passivation layer of matching work function with that of the glass plate surface. The Rdc charge could also be compensated by offset of common voltage. The voltage holding capability of the LC cell was determined by a depolarization field of molecules in the LC cell, and could be improved with a LC mixture of high specific resistivity. A minimal specific resistivity of 5×10^{12} Ω cm was required to maintain more than 97% VHR of the LC cell. The voltage holding capability of the silicon panel was determined primarily by temperature and secondarily by light leakage. A good light shield and room temperature were required to improve the VHR of the silicon panel. The parasitic capacitor coupling could also contribute to the flicker. A minimal parasitic to storage capacitance ratio of 80 was required to minimize the coupling effect. Imbalance driving was useful to compensate for parasitic capacitance coupling. Finally, frame rate multiplication was found very useful to minimize the flicker due to low VHR of the LC cell or silicon panel.

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