Active-Matrix Organic Light-Emitting Diode Displays Realized Using Metal-Induced Unilaterally Crystallized Polycrystalline Silicon Thin-Film Transistors

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***Abstract*—Requirement on thin-film transistors, particularly in terms of current-drive and parameter uniformity, for active-matrix organic light-emitting diode displays, was analyzed. Metal-induced unilaterally crystallized polycrystalline silicon thin-film transistor technology was shown to satisfy such and other demands. Though pixel designs involving more transistors were certainly advantageous, appropriate biasing scheme allowed a simpler and larger aperture-ratio two-transistor design. As a demonstration, active matrices were fabricated and integrated with organic light-emitting diodes to make monochrome video display panels, each consisting of 120 rows and 160 columns.**

***Index Terms*—Active matrix, flat-panel display, metal-induced lateral crystallization, organic light-emitting diodes, polycrystalline silicon, thin-film transistors.**

I. Introduction

WHILE liquid-crystal display (LCD) is presently the dominant flat-panel display technology because of its mature manufacturing practice, it is far from ideal. Organic light-emitting diodes (OLEDs) [1] are being hotly pursued as alternative display elements because of their relative merits of being self-emitting, having large intrinsic viewing-angle and fast response. Furthermore, the fabrication of "all solid-state" OLED displays is significantly simpler than that of LCDs, requiring neither light-attenuating polarizers nor the equivalents of polymer alignment layers and liquid-crystal "fill" [2].

Present commercial OLED displays are mostly passive-matrix (PM) scanned (cell phones, personal digital assistants, etc.) or direct-current (DC) driven (simple gauge and instrumentation panels, etc.) [3]. In order to achieve a given luminance (L) averaged over a "frame" period (T_f), a higher current drive within a shorter "line" time $(\sim T_f/n)$ is required for PM displays

$$\frac{L_{\rm PM}}{L_{\rm DC}} \approx \frac{\gamma I_{\rm PM}}{\gamma I_{\rm DC}} = n \Rightarrow I_{\rm PM} \approx n I_{\rm DC} \tag{1}$$

where n is the number of scan lines and γ, the luminance current efficiency [4] is assumed to be bias-independent. $I_{\rm PM}$ and $I_{\rm DC}$ are the currents required, respectively, for PM and DC-driven displays. Since the current–voltage $(I$–$V)$ characteristics of OLEDs can be phenomenologically modeled by $I \propto V^{\beta} \Rightarrow V \propto I^{1/\beta}$ [5] where V is the applied voltage and β is a constant, the corresponding power dissipation $(P_{\rm PM}$ and $P_{\rm DC})$ can be compared

$$\xi \equiv \frac{P_{\rm PM}}{P_{\rm DC}} = \frac{\frac{1}{n} I_{\rm PM} V_{\rm PM}}{I_{\rm DC} V_{\rm DC}} = \frac{1}{n} \left(\frac{I_{\rm PM}}{I_{\rm DC}} \right)^{1+1/\beta} = n^{1/\beta}. \tag{2}$$

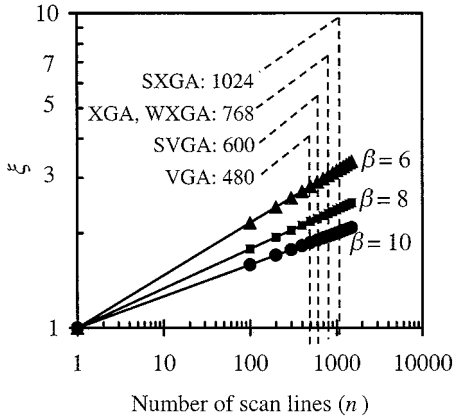

Fig. 1. Dependence on the number of scan lines (n) of the ratio (ξ) of the power dissipation of PM-driven to DC-driven displays at three different values of $\beta = 6$, 8 and 10.

Relative to that of an AM-OLED display, the power dissipation of a PM-OLED display increases with increasing n. The rate of increase of ξ is a function of β (Fig. 1). Besides the higher relative power consumption, it is known that the lifetime of an OLED reduces when driven at a higher current level [6], thus adversely affecting the long-term reliability of the resulting display. Therefore, while PM addressing scheme may be acceptable for small pixel-count matrix displays because of its simplicity, it is not suitable for television sets or high information-content monitors with significantly larger number of scan lines.

A better way of driving high information-content OLED displays is active-matrix (AM) addressing with "pixel memory" [7], [8]. The voltage stored on a "memory" capacitor maintains the desired diode current (hence the pixel brightness) throughout T_f, thus making the driving of the pixel effectively DC. Elimination of the high-amplitude current pulses

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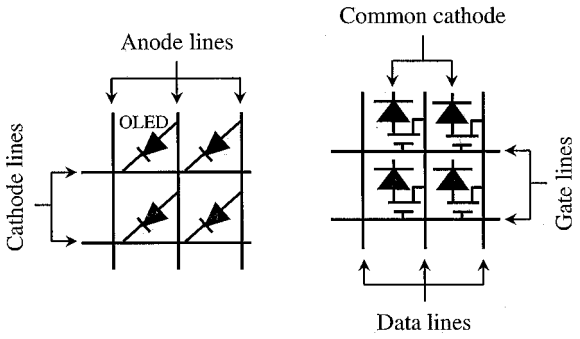

Fig. 2. Memory-less pixel configurations in (a) PM-OLED and (b) one-TFT AM-OLED displays.

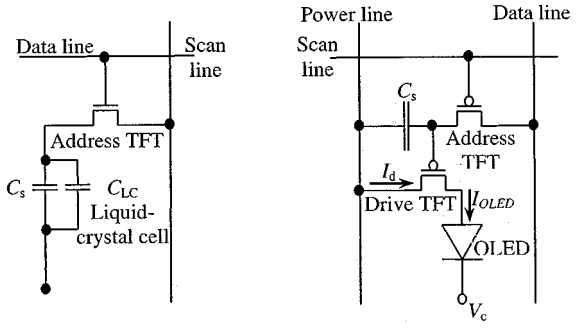

Fig. 3. Circuit schematics of active-matrix pixels of (a) LC and (b) OLED displays.

required for memory-less, scanned driving schemes such as transistor-less PM or single-transistor AM addressing (Fig. 2) results in both reduction in power dissipation and increase in display lifetime.

II. Transistor Technology Requirements

Unlike the optical state of a liquid-crystal pixel that can be voltage-switched using a single "address" transistor [Fig. 3(a)], the current-controlled emission of an OLED pixel requires at least two transistors ("address" and "drive") and a storage capacitor (C_s) to maintain a continuous diode current [$I_{\rm OLED}$ in Fig. 3(b)] in the "emitting" state. While it is feasible to implement pixel transistors in AM-LCDs using amorphous silicon (a-Si) thin-film transistors (TFTs) with relatively poor device characteristics, p-type polycrystalline silicon (poly-Si) TFTs capable of significantly higher current-drive are required for implementing pixel transistors in AM-OLED displays [9]–[11].

The variations of TFT device parameters directly affect the uniformity of OLED emission intensity. The sensitivity of the latter to the former depends on whether the drive TFT is biased in the saturation or the linear regime of operation. In the saturation regime, the drain current (I_d) is given by

$$I_d = \frac{1}{2}\mu_{\rm FE}C_{ox}\frac{W}{L}(V_{gs}-V_T)^2 \tag{3}$$

where $\mu_{\rm FE}$ is the field-effect mobility, C_{ox} is the gate oxide capacitance, W and L are the respective channel width and length of the TFT, V_{gs} is the applied gate-to-source voltage, and V_T is the threshold voltage. Acting as a current source, the TFT clearly controls $I_{\rm OLED}$, which can be varied to implement a desired grayscale. In this case, emission nonuniformity is dominated by parameter variations of the TFTs and relatively insensitive to those of the OLEDs. Consider only $\delta\mu_{\rm FE}$ and δV_T, but not δW or δL, the variation in drain current (δI_d) is given by

$$\left|\frac{\delta I_d}{I_d}\right|_{sat} \approx \left|\frac{\delta\mu_{\rm FE}}{\mu_{\rm FE}}\right| + 2\left|\frac{\delta V_T}{V_{gs}-V_T}\right|. \tag{4}$$

While the sensitivity to δV_T can be reduced by dynamically sampling V_T of the drive TFT using a four-TFT pixel design [12], reduction of the sensitivity to $\delta\mu_{\rm FE}$ is not as straight forward.

For a TFT operating in the linear regime with gate drive $(V_{gs}–V_T) \gg$ drain-to-source voltage (V_{ds})

$$I_d \approx \mu_{\rm FE}C_{ox}\frac{W}{L}(V_{gs}-V_T)V_{ds} \tag{5}$$

$$\Rightarrow \left|\frac{\delta I_d}{I_d}\right|_{lin} \approx \left|\frac{\delta\mu_{\rm FE}}{\mu_{\rm FE}}\right| + \left|\frac{\delta V_T}{V_{gs}-V_T}\right| + \left|\frac{\delta V_{ds}}{V_{ds}}\right|. \tag{6}$$

Assuming $I_{\rm OLED} = B(V_{ds}-V_{cs})^{\beta}$, where B is a proportionality constant and V_{cs} is the potential difference between the cathode of the OLED and the source of the TFT, it can be derived that

$$\left|\frac{\delta I_{\rm OLED}}{I_{\rm OLED}}\right| = \beta\left|\frac{\delta V_{ds}}{V_{ds}-V_{cs}}\right| \approx \beta\left|\frac{\delta V_{ds}}{V_{cs}}\right| \Rightarrow \left|\frac{\delta V_{ds}}{V_{ds}}\right| \approx \frac{1}{\beta}\left|\frac{V_{cs}}{V_{ds}}\right|\left|\frac{\delta I_{\rm OLED}}{I_{\rm OLED}}\right| \tag{7}$$

where it has been assumed that $|V_{cs}| \gg |V_{ds}|$. Because of current continuity [Fig. 3(b)], $I_{\rm OLED} = I_d$. Therefore

$$\left|\frac{\delta V_{ds}}{V_{ds}}\right| \approx \frac{1}{\beta}\left|\frac{V_{cs}}{V_{ds}}\right|\left|\frac{\delta I_{\rm OLED}}{I_{\rm OLED}}\right| = \frac{1}{\beta}\left|\frac{V_{cs}}{V_{ds}}\right|\left|\frac{\delta I_d}{I_d}\right|_{lin}. \tag{8}$$

Substituting (8) in (6), we have

$$\left|\frac{\delta I_d}{I_d}\right|_{lin} \approx \left|\frac{\delta\mu_{\rm FE}}{\mu_{\rm FE}}\right| + \left|\frac{\delta V_T}{V_{gs}-V_T}\right| + \frac{1}{\beta}\left|\frac{V_{cs}}{V_{ds}}\right|\left|\frac{\delta I_d}{I_d}\right|_{lin} \tag{9}$$

$$\Rightarrow \left|\frac{\delta I_d}{I_d}\right|_{lin} \approx \beta\left|\frac{V_{ds}}{V_{cs}}\right|\left(\left|\frac{\delta\mu_{\rm FE}}{\mu_{\rm FE}}\right| + \left|\frac{\delta V_T}{V_{gs}-V_T}\right|\right) \prec\prec \left|\frac{\delta I_d}{I_d}\right|_{sat} \tag{10}$$

where it has been assumed that $|V_{cs}| \gg \beta|V_{ds}|$. If TFT rather than OLED parameter variations dominated emission uniformity, biasing the drive TFT in the linear regime would be preferred. In fact, the effects of I_d variation can be minimized if $|V_{ds}|$ can be made arbitrarily small. For a given I_d, the lower bound for $|V_{ds}|$ is limited by how large $\mu_{\rm FE}$ is.

Consider, for example, a TFT technology with an oxide thickness of 100 nm, transistor dimensions of $W/L = 10\ \mu$m/5 μm and a gate drive $|V_{gs}-V_T| = 10$ V, a $\mu_{\rm FE}$ of 18.5 cm^2/Vs would be required to achieve an $|I_d|$ of 1.32 μA at a $|V_{ds}|$ of 0.1 V for a brightness of 100 cd/m^2 (assuming a γ of 6.8 cd/A, see Fig. 8) from a 300-by-300 μm^2 pixel. Because displays are usually implemented with the anodes of the OLEDs connected to the AM panels, p-type TFTs are normally used. Such high $\mu_{\rm FE}$ for holes cannot be obtained from an a-Si TFT. Even higher $\mu_{\rm FE}$ is desired, if parasitic TFT power dissipation and the effects of

TFT parameter variations on emission nonuniformity are to be minimized.

While high $\mu_{\rm FE}$ and small TFT parameter variation dominate concerns in the "on" state, leakage-current must be low enough in the "off" state of an address TFT to maintain the state of a pixel when not being addressed and in the "off" state of a drive TFT to maintain a high contrast ratio. The former typically presents a more stringent requirement. Take the example of a pixel with a total "memory" capacitance of $C_{\rm hold}$, the leakage-current induced time-variation in the signal voltage (V_s) held on $C_{\rm hold}$ can be modeled by

$$V_s = V_p e^{-(T/\tau_{\rm off})} = V_p e^{-(T/R_{\rm off}C_{\rm hold})} \Rightarrow R_{\rm off} = \frac{T}{C_{\rm hold} \ln \frac{V_p}{V_s}} \quad (11)$$

where V_p is the initial "drive" voltage "written" into the pixel, $\tau_{\rm off}$ and $R_{\rm off}$ are the respective effective time constant and resistance of the address TFT in the off-state and time $(T) \sim T_f$. For a 60-Hz frame frequency, $T_f \sim 16.7$ ms. Assuming a $C_{\rm hold} \sim 0.8$ pF and a 5% tolerance (i.e., $|V_s| \geq 0.95|V_p|$ at T_f) for the reduction in V_s, a value of $R_{\rm off} \geq 0.4$ GΩ can be estimated. If V_p is 5 V, the maximum leakage current is $\sim$2.5 pA/μm for a 5-μm-wide address TFT.

Regular transmissive type AMOLED displays are implemented on inexpensive glass substrates normally used also for LCDs. Therefore, the maximum process temperature for the desired poly-Si TFT technology must be lower than the strain points (e.g., 666 °C for Corning 1737) of the corresponding glass substrates. It is presently shown that low-temperature (LT) metal-induced unilaterally crystallized (MIUC) poly-Si TFT technology [13], with a process temperature not exceeding 550 °C, is capable of meeting the stringent specifications outlined above for AM-OLED displays.

III. LT MIUC Poly-Si TFT Technology

Poly-Si with large crystallite grains has been obtained using a variety of techniques: rapid thermal annealing (RTA) [14], excimer laser crystallization (ELC) [15], and solid-phase crystallization (SPC) [16]. RTA is a high temperature (>600 °C) process, resulting in films containing high densities of defects. By localizing the high temperature to the silicon layer, ELC can be considered a "low" temperature process. While it is capable of producing poly-Si films with low defect densities, it suffers from high initial cost and high process complexity. Conventional SPC is a relatively inexpensive batch process, though at around 600 °C, the processing temperature is still considered high.

Metal-induced laterally crystallized (MILC) poly-Si technology is a process of forming poly-Si using the technique of nickel (Ni)-induced crystallization of a-Si at a glass-compatible temperature of no more than 550 °C [17]. With the crystallization-inducing window confined to one end of the active island, MIUC poly-Si TFT technology is a batch-fabrication device technology based on the MILC poly-Si material technology. Schematic cross-sectional diagrams showing the evolution of the structure of an MIUC TFT under construction are shown in Fig. 4. The corresponding device characteristics are summarized in Table I.

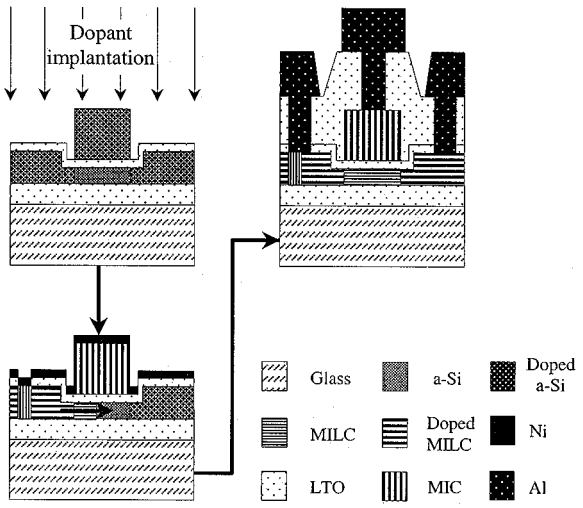

Fig. 4. Schematic cross-sectional diagrams showing the evolution of the structure of an MIUC TFT under construction.

TABLE I
Device Parameters of n- and p-Channel LT MIUC Poly-Si TFTs. V_{bd} is the Drain-to-Source Breakdown Voltage

	N-type	P-type
$\mu_{\rm EF}$ (cm^2/Vs)	121	108
$V_{\rm T}$ (V) $\lvert V_{\rm ds}\rvert$=5V	3.2	-4.5
S (V/decade)	1.1	1.0
$V_{\rm bd}$ (V)	20	-55
$I_{\rm off}$ (pA/μm) $\lvert V_{\rm d}\rvert$=5V	4.8	3.2
$I_{\rm on}$ (μA/μm) $\lvert V_{\rm d}\rvert$=5V	33	33

At around 100 cm^2/Vs, the high $\mu_{\rm FE}$ for both electrons and holes are more than adequate for driving OLEDs. Indeed, such high values can be advantageously exploited to reduce parasitic TFT power dissipation and to minimize TFT parameter variation induced brightness nonuniformity. Both low V_T and small subthreshold slope (S) help reduce the required V_{gs} to achieve a given V_{gs}–V_T, thus reducing also the power consumption of the display. The leakage current $(I_{\rm off})$ in the "off" state, at 3.2 pA/μm, is marginal but usable. Though it can be further reduced by incorporating commonly exploited structures such as off-set drain [18], lightly doped-drain [19] or gate-overlapped drain with MILC process optimization [20].

Because of the unique microstructure of MILC poly-Si, the relative variations of MIUC TFT device parameters are significantly smaller than those of the other poly-Si TFTs [12]. In the present implementation, $\delta\mu_{\rm FE}$ are 15 cm^2/Vs and 12 cm^2/Vs [Fig. 5(a)], respectively, for electrons and holes. A δV_T of $\sim$0.6 V [Fig. 5(b)] is obtained for both n- and p-type MIUC TFTs. With a $\mu_{\rm FE}$ of $\sim$108 cm^2/Vs (Table I) for p-type TFTs and a $|V_{gs} - V_T| = 10$ V, one obtains $|\delta I_d/I_d|_{\rm sat} \approx 0.23$. This is equivalent to a maximum grade level of $\sim$4. Assuming

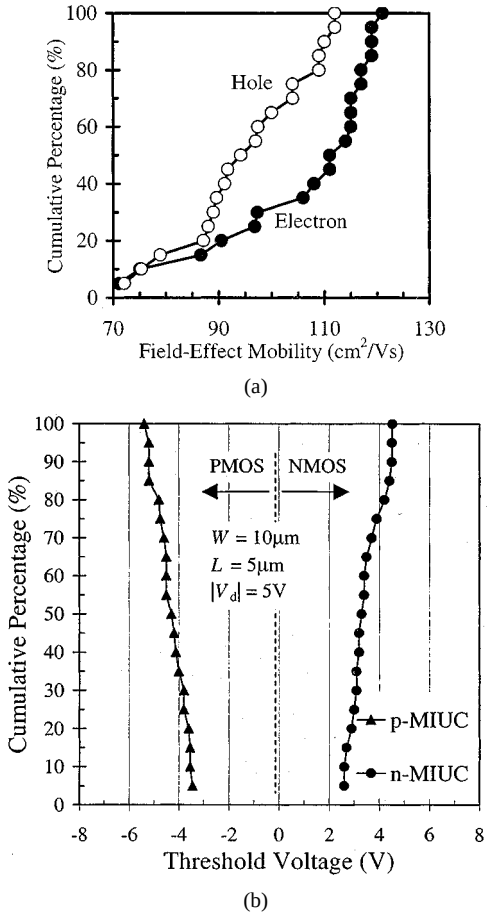

Fig. 5. Statistical distributions of (a) $\mu_{\rm FE}$ and (b) V_T of n- and p-channel LT MIUC TFTs.

a β of 10, a $|V_{ds}|$ of 0.05 V and a $|V_{cs}|$ of 10 V, one obtains $|\delta I_d/I_d|_{lin} \approx 0.01$. This is potentially equivalent to ~100 gray levels.

Though the potential number of gray levels is large, the dynamic range of brightness control is small because almost the entire supply voltage is dropped across the OLED. In this case, gray-scale control in the linear regime of operation is best accomplished using either area dithering or pulse width modulation. Instead of acting like a current source as in the saturation regime of operation, the drive TFT functions simply as a digital switch [2], [21].

IV. AM-OLED TFT Panel Fabrication

A conventional OLED structure was adopted in the present work, with the indium–tin oxide (ITO) anode deposited first, the various OLED constituent organic layers formed next and the reflective metallic cathode cap layer deposited last. Because of the low tolerance of the constituent organic materials to high temperature processing, construction of AM-OLED display must follow the sequence of first finishing the fabrication of the MIUC TFTs before implementing the OLEDs [22].

Corning 1737 glass was used as the starting substrates, preshrunk for 60 h at 630 °C. Consequently, a further shrinkage of lower than 5 ppm was induced at the end of the TFT fabrication process. Panel fabrication started with the low-pressure chemical vapor deposition (LPCVD) of 800 nm insulating low-temperature oxide (LTO) at 425 °C. A 100 nm LPCVD a-Si layer was deposited at 550 °C and patterned to form the "thick" source and drain (S/D) islands. This was followed by the deposition and patterning of a thinner 30 nm LPCVD a-Si active layer [23].

The gate-stack consisted of a 100-nm LTO insulator and 280-nm a-Si electrode. After the gate electrode definition, 40 keV boron ions at a dose of 4×10^{15}/cm^2 were implanted for self-aligned gate and S/D doping. Prior to MIUC, small windows were opened through the LTO on selected junctions of the TFTs and 5-nm-thick Ni was deposited in a high-vacuum electron-beam evaporator. While the gate was metal-induction crystallized (MIC), the channel region was laterally crystallized at a rate of 4–5 μm/h at 500 °C in nitrogen. During the crystallization, the implanted boron was simultaneously activated.

Any unreacted Ni was subsequently removed in heated sulfuric acid. An insulating layer of 300-nm LTO was next formed and contact holes opened to the gate electrode. Subsequently, a layer of 300-nm titanium was deposited and patterned to provide not only a low-resistance shunt to the relatively highly resistive MIC poly-Si gate, but also a yield-enhancing redundant interconnect level. Contact holes were opened through a 600-nm LTO interlevel dielectric layer before Al–1%Si alloy was sputter-deposited and patterned to form the interconnections. Final sintering was performed for 30 min at 420 °C in forming gas.

V. OLED Integration

OLED fabrication began with the deposition of 500 nm plasma-enhanced CVD oxide and the opening of via holes to Al–1%Si. A liftoff photoresist mask was then defined prior to the room temperature sputtering of 100-nm ITO transparent electrode. Following the liftoff process, a 2-μm-thick polymer insulation layer was coated and through which anode openings, each smaller than the size of the corresponding ITO electrode, were formed. The polymer served to improve the interlevel insulation, to reduce the parasitic capacitance and to minimize the detrimental effects of the strong electric field emanating from the edges of the ITO electrode. The edges of the polymer opening were also smoothed to improve the coverage of the subsequently evaporated organic layers. Exposed ITO was cleaned and treated with ozone under ultraviolet illumination for 5 min before loading into the vacuum chamber for the deposition of the organic layers.

At an initial pressure of 20 μtorr, 20 nm copper (II) phthalocyanine (CuPc) anode buffer layer, 50 nm 5% rubrene doped N,N′-diphenyl-N,N′-bis (3-methylphenyl) 1,1′-bipheny-4,4′ diamine (TDP : Ru) hole transport layer and 60 nm *tris*-8-hydroxy–quinoline aluminum (Alq_3) electron transport layer were sequentially evaporated through appropriately designed shadow masks. The various organic films were deposited at rates of ~0.2 nm/s. The final reflecting cathode layer consisted of 1-nm lithium fluoride (LiF) capped with 150 nm Al. The devices were encapsulated in nitrogen using glass covers. A cross-sectional schematic of an OLED pixel is shown in Fig. 6.

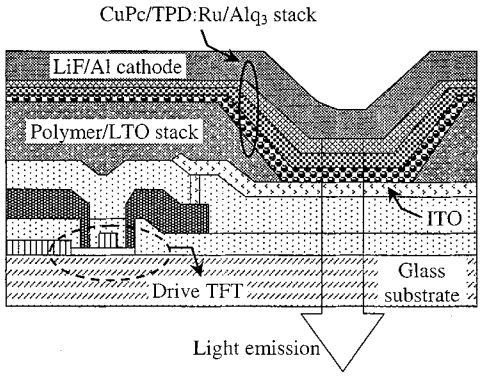

Fig. 6. Schematic cross-section of an OLED, showing the constituent organic thin films.

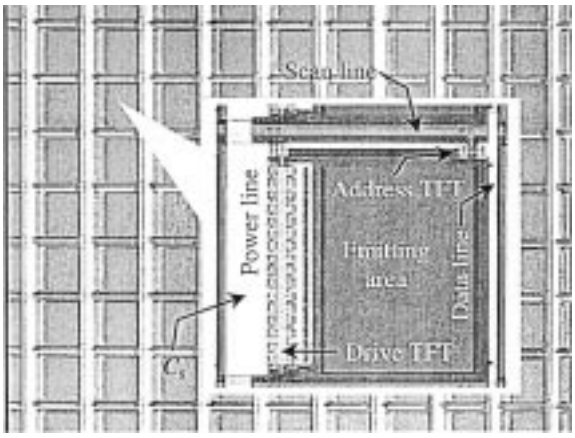

Fig. 7. Photograph showing a portion of the finished 120 × 160 AM-OLED pixel matrix and a magnified pixel showing the various electronic components and interconnects.

VI. AM-OLED Display Characteristics

The 6.6 cm-diagonal display matrix consists of 120 rows by 160 columns on transparent glass substrates. Each pixel (Fig. 7) is made up of an OLED, the anode of which is connected to the drain of a drive TFT with a large $W/L = 250\ \mu$m/5 μm for minimal parasitic TFT power dissipation. The state of this TFT is controlled by a smaller address TFT ($W/L = 3/5\ \mu$m). The voltage signal is held on a storage capacitor ($C_s \sim 0.8$ pF) formed between the gate of the drive TFT and the Al power interconnect.

Typical "luminance (L)-current density (J)-voltage (V)" characteristics of an OLED is shown in Fig. 8. A maximum brightness of 27 000 cd/m^2 was obtained at an OLED forward bias of 15 V. The corresponding power efficiency is ~1.5 Lm/W.

The display was driven using a custom-designed PAL analog driver board. An operating point in the linear operating regime of the drive TFT at the maximum brightness was selected to minimize the effects of TFT parameter variations. The address TFT was turned off and on at 0 V and −15 V, respectively. The data (column) voltage transferred by the address TFT and stored on C_s was varied continuously between a maximum of 0 V and a minimum of −7 V to control $I_{\rm OLED}$ delivered by the drive TFT. The voltage levels on the source of the drive TFT (which was attached to the power line) and the cathode of the OLED were 5 and −5 V, respectively.

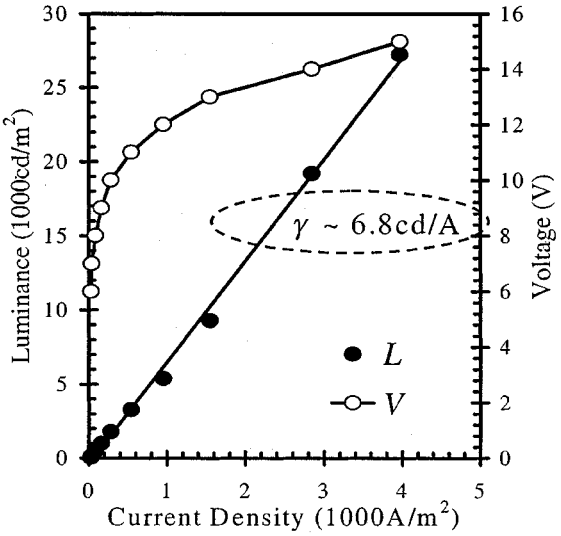

Fig. 8. Typical OLED L–J–V characteristics. A luminance current efficiency (γ) of 6.8 cd/A is extracted from the L–J dependence.

Fig. 9. A representative image captured from the monochrome AM-OLED display.

Since the source of the drive TFT is attached to the power line, which is biased at 5 V, and $V_g = -7$ V is used to turn on the drive TFT, therefore, V_{gs} on the drive TFT is −12 V. Consequently, $V_{gs} - V_T = -7.5$ V, in which $V_T = -4.5$ V (Table I) for p-type MIUC TFT is used. Assuming a γ of 6.8 cd/A (Fig. 8), an $I_{\rm OLED}$ of ~2 μA is needed for a pixel brightness of 150 cd/m^2. This is equivalent to a $|V_{ds}|$ of ~15 mV. Since $|V_{ds}| \ll |V_{gs} - V_T|$, the drive TFT is biased in the linear regime of operation.

A typical image captured from a monochrome AM-OLED video display is shown in Fig. 9. The average luminance in the bright state was ~150 Cd/m^2, with a relative variation less than 7.5%. More than eight levels of gray scale were achieved. As expected, large viewing-angle and video-rate compatible fast switching response were obtained. The maximum power dissipation was 200 mW, low enough to avoid excessive heating of the panel during extended operations.

Clearly, the display as implemented is far from perfect, exhibiting both line and point defects. Some of the defects resulted from the active matrix and some from the OLEDs. The

non-emitting horizontal "line defect" is caused by shorting of a scan line to the power line. The non-emitting vertical "line defect" is caused by shorting of a data line to the power line. The gate voltage levels of the TFTs on the affected rows and columns were permanently stuck at the "off" polarity of 5 V. These line defects originate from the active matrix.

Bright "point defects" are caused by shorts between the power lines and the ITO anodes, thus bypassing the drive TFTs. Consequently, the affected OLEDs are always on because of the permanent full 10 V forward drop across the diodes. Dark "point defects" are mainly caused by malfunctioning OLEDs, either resulting from delamination of the cathode metal from Alq_3 or shorting of anode and cathode electrodes.

VII. Conclusion

Thin-film transistor requirements, particularly in terms of current drive and parameter uniformity, for active-matrix organic light-emitting diode displays, have been analyzed. Metal-induced unilaterally crystallized polycrystalline silicon thin-film transistor technology has been shown to satisfy such and other demands. Issues related to the integration of organic light-emitting diodes and the underlying thin-film transistor active matrix have been explored. As a demonstration, active matrices were fabricated and integrated with organic light-emitting diodes to make monochrome display panels, each consisting of 120 rows and 160 columns.

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