P-1: Peripherally Crystallized Polycrystalline Silicon (PCP) for Thin-Film Transistors

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ABSTRACT

Metal-induced peripheral crystallization is proposed and demonstrated as an alternative scheme based on the general technique of metal-induced lateral crystallization of amorphous silicon. Compared to the scheme of unilateral crystallization, peripheral crystallization requires a shorter process time and reduced masking step. Compared to the scheme of self-aligned bilateral crystallization, it largely retains the better material and device properties of unilateral crystallization.

1. INTRODUCTION

Low temperature crystallization of amorphous silicon (a-Si) thin film has attracted considerable attention because of its potential applications to large area electronics on inexpensive glass substrates. Thin-film transistors (TFTs) built on metal-induced laterally crystallized (MILC) polycrystalline silicon (poly-Si) have been shown to exhibit high carrier mobility, good device uniformity and simple fabrication process. They can be used to realize active-matrices [1, 2] for flat-panel display and image sensor applications [3-7].

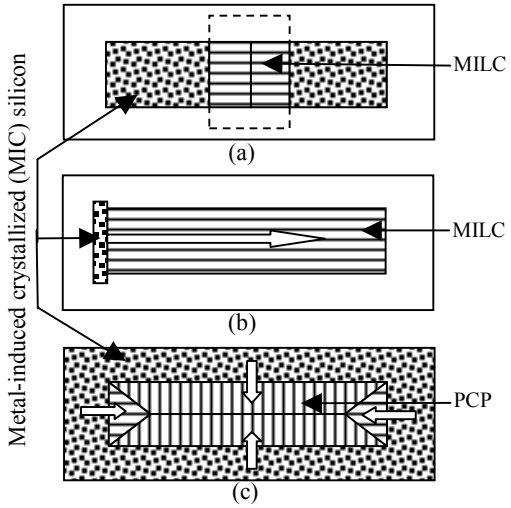

Figure 1. Schematics of active islands formed using different schemes of crystallization: (a) MILC self-aligned to the channel edge; (b) Lateral crystallization with additional nickel window; (c) PCP.

Two popular implementations are (Fig. 1a) MILC with nickel (Ni) coverage self-aligned to the edges of a TFT channel [6] and (Fig. 1b) unilateral crystallization with the definition of an extra Ni window [8, 9]. Compared to the former, the latter requires an additional photolithography step and a much longer crystallization time, but results in better material quality and device performance.

A new implementation scheme (Fig. 1c), leading to peripherally crystallized polycrystalline silicon (PCP), is presently proposed. While largely retaining the material and device advantages of unilaterally crystallized polycrystalline silicon (poly-Si), PCP requires no extra photolithography step for defining any Ni window and a short crystallization time comparable to the self-aligned MILC scheme.

2. Fabrication of PCP TFT

The realization of PCP starts with sequential depositions of low-temperature oxide (LTO) on a-Si. This is followed by the definition of an LTO Ni mask after the usual active-island photolithography step. Ni is subsequently deposited and crystallization induced at 550^{o}C. Since MILC proceeds from the entire periphery of an island (Fig. 2a), the time required for its complete crystallization is

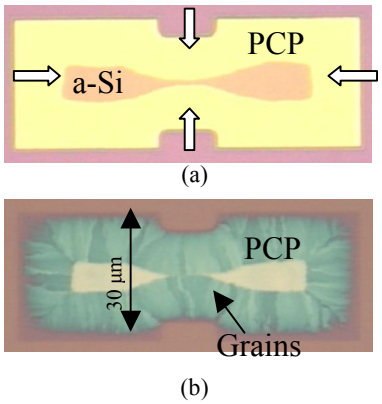

Figure 2. (a) PCP active island after MILC process, yellow region is MILC poly-Si and brown region is a-Si; (b) Large size crystal grains within the active island is observed after removal of the top 25nm silicon by wet-etching.

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significantly reduced compared to that required by the unilateral crystallization scheme. Active islands are formed by removing all exposed silicon outside the LTO-covered region. Shown in Figure 2b is a PCP island after wet etching the top 25nm of silicon. The grain texture is enhanced and 2-7μm crystal grain can be observed. The crystallization time for wider transistors can be reduced by dividing the channels into a collection of narrower channels, as schematically shown in Figure 3.

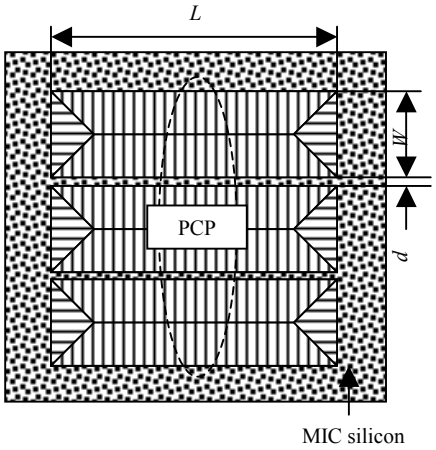

Figure 3. Schematic of a wide channel formed by combining three narrower PCP channels.

Following the active island definition, LTO was deposited as gate oxide. Subsequently, poly-Si was deposited as gate electrode, which was followed by gate patterning, self-aligned gate, source and drain implantation, and subsequent dopant activation. An LTO insulation layer was deposited before opening contact holes and forming aluminum electrodes. The schematic cross section of a completed PCP TFT is shown in Figure 4. Relevant geometric and process parameters of the PCP TFTs are summarized in Table I.

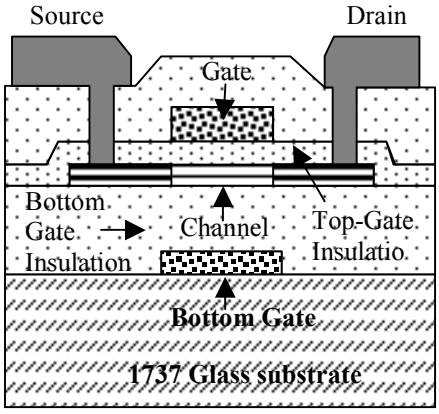

Figure 4. Schematic cross-section of a PCP TFT with an auxiliary bottom gate.

Table I. Geometric and process parameters of the PCP TFTs.

Bottom Gate	**200nm doped poly-Si**
Bottom Gate Oxide	**500nm LPCVD LTO**
Active Layer	**50nm LPCVD a-Si** **MILC heat treatment: 550℃ for 3hrs**
Top Gat Oxide	**125nm LPCVD LTO**
Top Gate Electrode	**300nm poly-Si**
Doping	**Boron/phosphorus: 40/120KeV. Dosage: $4x10^{15}/cm^2$**
Insulation Layer	**500nm LPCVD LTO**
Doping Activation	**600℃, 3hrs**
Metal Electrode	**500nm sputtered Al**

3. Results and Discussion

The threshold voltage (V_{th}) of PCP TFT is found to depend on TFT channel width (W), as shown in Figure 5. This dependence originates from charge traps in the continuous longitudinal grain boundary, located in the middle of the channel and runs from the source to the drain. It can be advantageously used to adjust the V_{th} of PCP TFTs. If the dependence is considered undesirable, it can be reduced by channel doping or laser annealing. Because of the absence of such longitudinal grain boundary in unilaterally crystallized poly-Si, similar dependence is not observed in the corresponding TFTs.

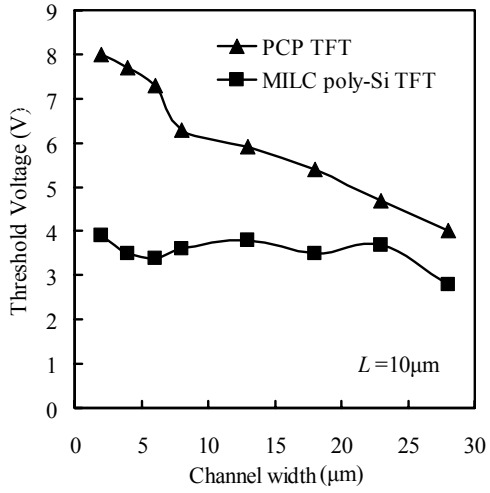

Figure 5. Channel width dependence of threshold voltage of PCP and MILC poly-Si TFTs.

With an additional mask, an auxiliary bottom gate (Fig. 4) can be implemented to improve the control of transistor behavior. A constant bias is applied to the bottom gate to provide a desired shift to V_{th}. The parasitic capacitance

between the channel and the bottom gate can be made small by thickening the bottom insulator (Table 1).

Electrically biasing the bottom gate is a more flexible way of controlling V_{th}. This leads to process simplification by eliminating the photolithography steps required for different threshold-adjust implants. The dependence of the transfer characteristics on bottom gate bias is shown in Figure 6. A V_{th} shift of about 5V is achieved. Furthermore, by turning off the "back channel" leakage path, a ~10 times reduction in the off-current (I_{off}) is obtained.

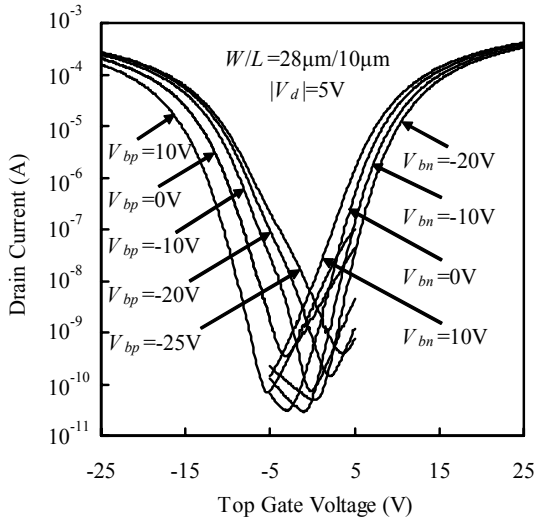

Figure 6. Bottom-gate voltage dependence of the transfer charateristics of PCP TFTs. V_{bn} and V_{bp} stand for bottom gate voltage of n- and p-type devices, respectively.

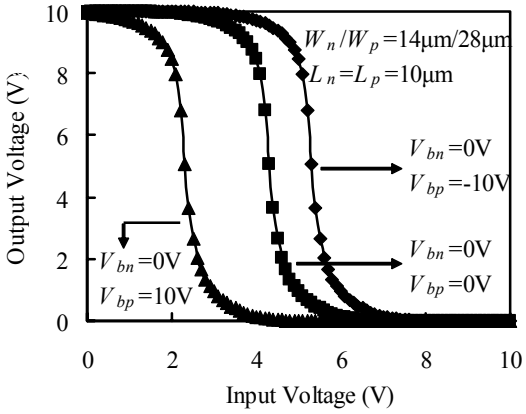

Figure 7. Voltage transfer characteristics of inverters constructed using PCP TFTs with different DC voltage on the bottom-gate.

As a demonstration of the utility of the bottom gate bias, typical voltage transfer characteristics of an inverter using n-type pull-down and p-type pull-up TFTs are shown in Figure 7. At a bottom gate bias of 0V, the transfer characteristic is not symmetrical. Clearly, the symmetry can be improved by maintaining 0V for the bottom gate of the n-type TFT but applying a negative voltage to the bottom gate of the p-type TFT.

Typical transfer characteristics of n- and p-type TFTs are shown in Figure 8. The bottom gate is biased at 0V. Respective field-effect mobility values (μ_{FE}) of ~87cm^2/Vs and ~61cm^2/Vs are obtained for electrons and holes. An on-current (I_{on}) to I_{off} ratio of over ~10^7 is obtained, at a drain bias (V_d) of 5V. Further decrease in I_{off} and increase in on-off ratio can be realized using an alternative device structure, as shown in Figure 9 for single- and double-gate TFTs with equivalent W and channel length (L). Not surprisingly, I_{off} of a double-gate TFT shows reduced dependence on V_d, particularly for V_d > 8V.

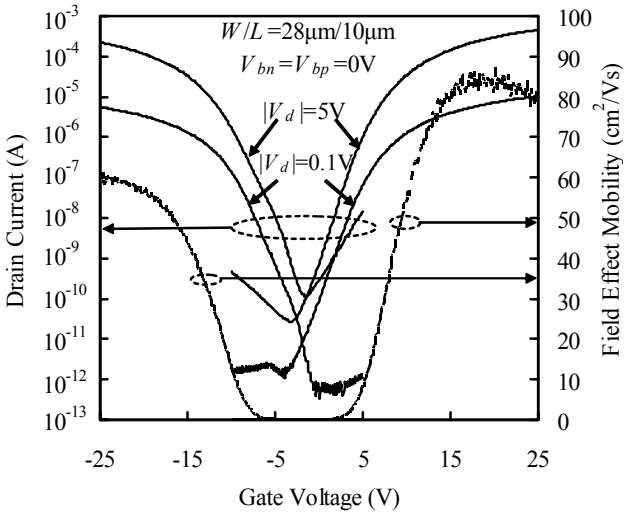

Figure 8. Transfer characteristics of n- and p-type PCP TFTs at V_d=0.1 and 5V.

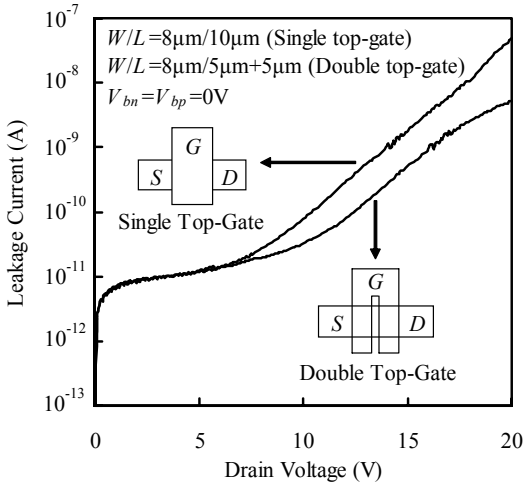

Figure 9. The drain voltage dependence of the leakage current of single and double top gate PCP TFTs with equivalent channel lengths. *S*, *D* and *G* denote source, drain and gate, respectively.

Typical output characteristics of n- and p-type TFTs are shown in Figure 10. At "equal magnitude" gate bias (V_g) and V_d, the output current of an n-type TFT is ~3 times higher than that of a p-type TFT with identical geometries. Part of the enhancement is due to the higher electron μ_{FE}, and the rest is due to the smaller magnitude of V_{th} of an n-type TFT.

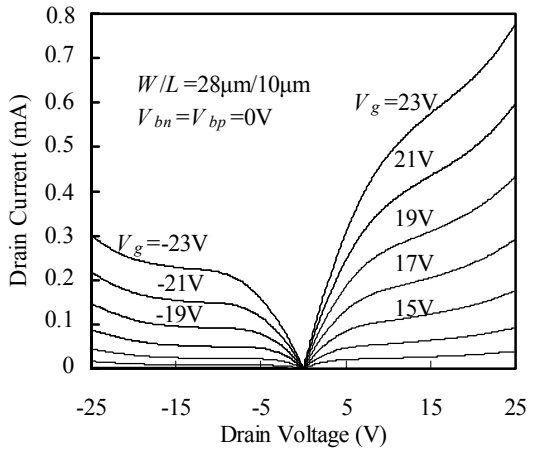

Figure 10. Output characteristics of n- and p-type PCP TFTs. At "equal magnitude" V_g and V_d, the output current of an n-type TFT is ~3 times higher than that of a p-type TFT with identical geometries.

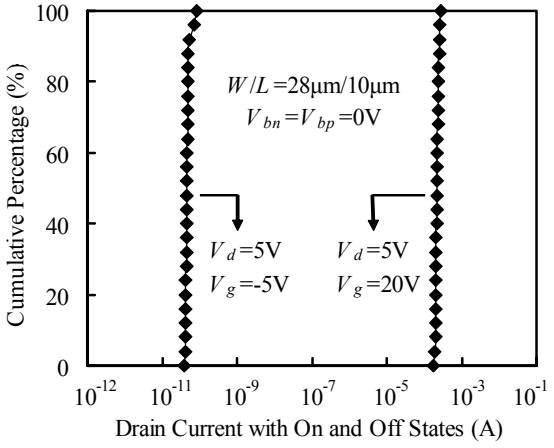

Figure 11. Statistical distribations of on- and off-state current of n-type PCP TFT at V_d=5V.

Parameter variation is of great concern for poly-Si TFTs. The cumulative distributions of I_{on} and I_{off} are shown in Figure 11. The respective standard deviations are 10.3% and 18.9%.

4. Conclusion

A new MILC scheme is presently proposed to realize metal-induced, peripherally crystallized polycrystalline silicon. This process retains the material and device advantages of unilateral MILC polycrystalline silicon, but requires a short crystallization time comparable to that of the self-aligned MILC scheme and no extra photolithography step. A bottom gate device structure is proposed to simplify processing and provide flexibility for threshold voltage control.

5. Acknowledgement

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