Polycrystalline Silicon Films and Thin-Film Transistors Using Solution-Based Metal-Induced Crystallization

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***Abstract*—Polycrystalline silicon (poly-Si) films consisting of dish-like and wadding-like domains were obtained with solution-based metal-induced crystallization (SMIC) of amorphous silicon. The Hall mobility of poly-Si was much higher in dish-like domains than in wadding-like domains. Thin-film transistors (TFTs) have been prepared using those two kinds of poly-Si films as the active layer, followed by the phosphosilicate glass (PSG) nickel gettering. The field effect mobility of dish-like domain poly-Si TFTs and wadding-like poly-Si TFTs were $70 \sim 80$ cm^2/V · s and $40 \sim 50$ cm^2/V · s, respectively. With a multi-gate structure, the leakage current of poly-Si TFTs was reduced by 1 to 2 orders of magnitude. In addition, the gate-induced drain leakage current (GIDL) and uniformity of the drain current distribution were also improved. P-type TFTs fabricated using SMIC exhibited excellent reliability.**

***Index Terms*—Metal-induced crystallization (MIC), nickel gettering, polycrystalline silicon (poly-Si), thin-film transistors (TFTs).**

I. Introduction

WHILE most active matrix liquid crystal displays (LCDs) are made of amorphous silicon (a-Si) thin-film transistors (TFTs), there is always a demand for polycrystalline silicon (poly-Si) based active matrix displays because the latter can provide much higher resolution and smaller pixels. As well, some of the driver circuitry can be integrated onto the glass substrate in the case of poly-Si TFT. Additionally, the p-Si TFT is more stable than a-Si TFT in terms of driving organic light emitting diode (OLED) displays. Thus low cost, high performance and reliable low temperature poly-Si (LTPS) processing technologies are greatly required [1], [2].

Poly-Si films with large crystalline grains have been obtained using the techniques of excimer laser annealing (ELA) [3] and metal-induced crystallization (MIC) [4]. There are several variations of MIC such as metal-induced lateral crystallization (MILC) and metal induced unilateral crystallization (MIUC). We shall refer to all of them as MIC in the following. ELA is capable of producing poly-Si films with low defect densities and high mobilities. However it suffers from high initial equipment cost, high maintenance cost, high process complexity and low device uniformity. MIUC poly-Si TFTs employing annealing at 550 °C has been studied [5]. Although capable of high performance and good uniformity, MIUC TFT needs an additional mask to define the crystallization-inducing windows, which makes the process more complicated and higher cost. Additionally, residual nickel in the poly-Si channel can affect the long term stability of the TFT. The electric performance of MIC TFT may shift and suffer higher off-state leakage current and early drain breakdown. So poly-Si TFTs with reduced fabrication complexity, high performance, reliability and uniformity is the key factor of its practicality [6].

There have been several attempts to reduce the Ni content in MIC based TFT. Dish-like poly-Si silicon has been obtained by Ni-mediated crystallization of a-Si with a silicon-nitride (SiN_x) cap layer [7]. In this process, Ni was sputtered onto the SiN_x/a-Si layer and then annealed at around 600 °C. The cap SiN_x controlled the Ni content inside the MIC layer to within tolerable levels. However, that process is quite complicated. It is also higher cost because of the vacuum process involved and the need to remove the cap layer afterwards.

In this paper, we shall discuss a solution-based MIC (SMIC) process for the fabrication of poly-Si TFT. Low Ni concentration is obtained by controlling the Ni adsorption process in the solution. This process can produce dish-like and wadding-like domains of poly-Si. It is the purpose of this paper to compare TFTs produced in these two types of domains. As well, the effect of phosphosilicate glass (PSG) gettering is investigated. Using optimized SMIC and PSG gettering, good performance, high uniformity and reliability poly-Si TFTs can be obtained.

II. SMIC Poly-Si Material

A. Preparation of SMIC Poly-Si Material

The fabrication process began with 4-in c-Si wafers covered with 500-nm thermal oxide. Then 50-nm a-Si active layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. After dipping in 1% hydrogen fluoride solution for 1 min to remove the native oxide, the sample was immersed in a 10-ppm (quality ratio of nickel nitrate crystalline to deionized water) nickel nitrate solution with a pH value of 8. The pH value

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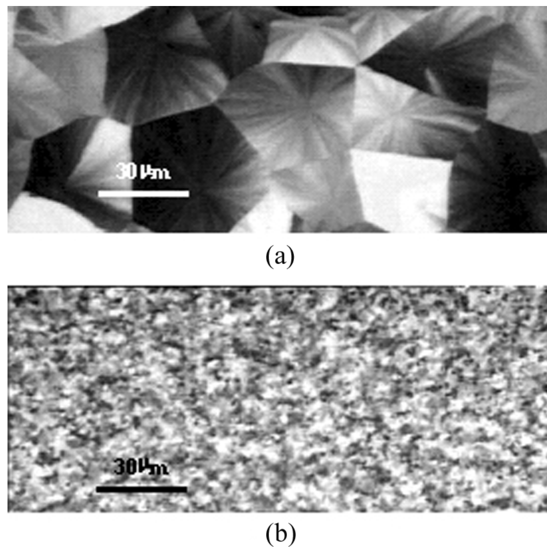

Fig. 1. Optical microscopy images of fully crystallized poly-Si etched by TMAH. (a) Disk-like domains and (b) wadding-like domains.

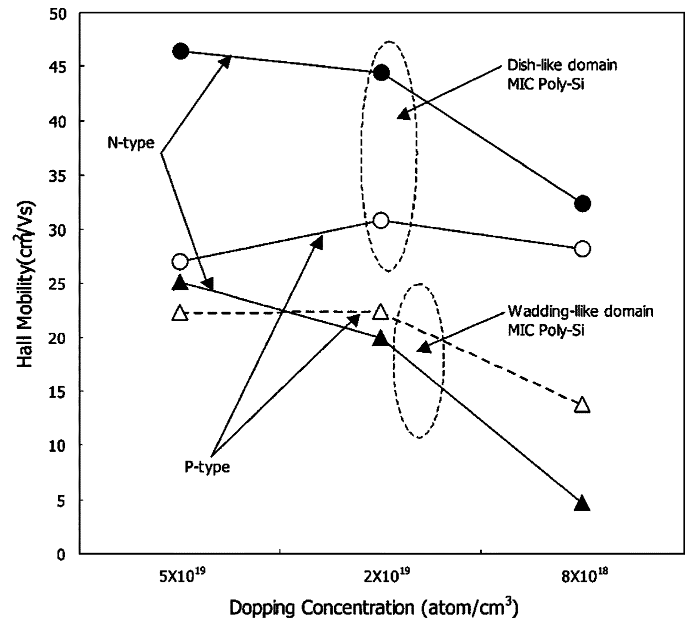

Fig. 2. Hall mobility of the disk-like domain and wadding-like domain poly-Si films.

was adjusted by adding a small amount of ammonia. The samples were then annealed at 590 °C for 4 hours together in nitrogen ambience and were fully crystallized. When the immersion time was 2 min, a yellow disk-like domain structure was observed on the film. The domains have a typical diameter of 10–15 μm, as shown in Fig. 1. When the immersion time was increased to 10 min, the domains became wadding-like, as shown in Fig. 1. Two types of domains were found in the poly-Si film between 2 and 10 min, for example, for 5 min. The effect of PSG gettering of nickel during the crystallization was also studied by depositing 700-nm PSG onto half of the wafer, followed by annealing at 590 °C for 4 h in nitrogen ambience.

The samples were cut into squares of 6 mm $\times$ 6 mm before phosphorus and boron implantation. Doses of 8×10^{13}, 2.0×10^{14} and 5×10^{14} atoms/cm^2 were used for various samples which were then post-annealed at 590 °C for 3 h for activation.

B. SMIC Poly-Si Material Analysis

Because of the etching selectivity of tetramethyl ammonium hydroxide (TMAH) etchant between different crystalline orientations, the etched poly-Si by TMAH at room temperature showed the inside structure of the films. The morphologies of SMIC poly-Si were studied using this technique. Two distinctly different kinds of structures were observed and shown in Fig. 1. They correspond to immersion times of 2 and 10 min, respectively. Fig. 1(a) shows the dish-like domains and the obvious colliding grain boundaries. The average domain size was about $30 \sim 50$ μm. The wadding-like domains and ambiguous grain boundaries were shown in Fig. 1(b), where the average domain size was about $3 \sim 5$ μm.

It was found that the Hall mobility of dish-like domain poly-Si was much higher than that of wadding-like domain poly-Si after activation. As shown in Fig. 2, the highest Hall mobility of p-type poly-Si which was obtained at an implantation dose was 1×10^{14} atoms/cm^2 (corresponding to 2×10^{19} atoms/cm^3) was 30.8 cm^2/V $\cdot$ s of dish-like domains and 22.5 cm^2/V $\cdot$ s for wadding-like domains, respectively. With the implantation dose increasing up to 2.5×10^{14} atoms/cm^2 (corresponding to 5×10^{19} atoms/cm^3), the Hall mobility decreased to 27.1 cm^2/V$\cdot$s for dish-like domains and 22.3 cm^2/V $\cdot$ s for wadding-like domains. From these results, it can be seen that the Hall mobility of dish-like p-type poly-Si was much higher than that of wadding-like domain poly-Si, and it decreased a little as the impurity concentration was increased. It can be confirmed that the dish-like domain poly-Si has better crystallization quality, lower defect density and less grain boundaries compared to wadding-like domain poly-Si [8].

For n-type SMIC poly-Si, its Hall mobility increased with the increasing of the impurity concentration when the impurity concentration was lower than 5×10^{19} atoms/cm^3. The Hall mobility of dish-like domain and wadding-like domain poly-Si was 46.5 cm^2/V $\cdot$ s and 25.2 cm^2/V $\cdot$ s respectively when the impurity concentration was 5×10^{19} atoms/cm^3. This result implies that defects and grain boundaries in the SMIC poly-Si has more effect on the motion of electrons than that of holes [9].

The sample immersed for 5 min was annealed at 550 °C for 3 h and 700-nm PSG was deposited and half of it was removed by wet etching, followed by a post-annealing at 590 °C for 4 h in nitrogen ambience. After the removal of the PSG layer by 777 etchant (composed of CH_3COOH, NH_4F and grycol) and etching with TMAH etchant, the grain structure was studied and is shown in Fig. 3. The circle in the domain center was the edge of crystalline disk after annealing at 550 °C for 3 hours, and the left half was the region not covered by PSG while the right part region was covered by PSG during the following annealing at 590 °C for 4 h. We can see that the SMIC crystallization length of the left part was as long as 60–70 μm, while the right part was only 15–17 μm after 590 °C 4 h annealing. The crystallization rate was much reduced as parts of nickel was gettered out by PSG during

TABLE I
SUMMARY OF RESULTS FOR SMIC TFT, MEASURED AT $|V_{ds}| = 0.1$ V AND $|V_{ds}| = 5$ V

	N-Channel				P-Channel			
	Type-A	Type-B	Type-C	Type-D	Type-A	Type-B	Type-C	Type-D
μ_{FE}(cm^2/Vs)	81.7	72.1	48.7	45.0	73.8	70.1	49.2	43.4
V_{th} (V)	10.3	10.5	14.0	14.3	-14.3	-13.0	-16.0	-15.0
S (V/ decade)	1.21	1.28	1.51	1.57	1.70	1.60	1.96	1.86
I_{off} (pA/μm) Minimum	1.32	1.37	1.06	0.95	1.55	1.50	1.19	1.0
I_{off} (pA/μm) $\|V_{ds}\|$=5V $\|V_{gs}\|$=10V	52.6	64.7	56.7	60.0	363.2	440.3	333.1	433.6
I_{on}/I_{off} (x10^7) $\|V_{ds}\|$=5V	1.66	1.49	0.94	1.11	1.02	1.01	0.7	0.82

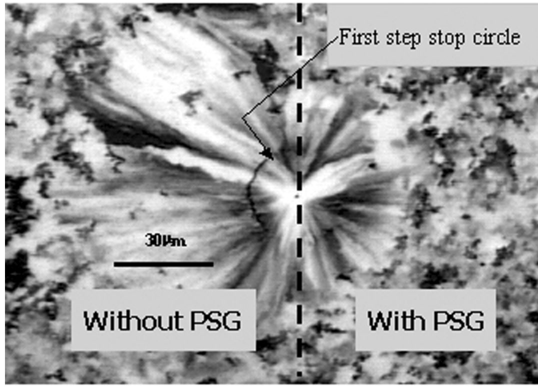

Fig. 3. PSG nickel gettering effect on SMIC poly-Si films.

the crystallization process. This confirmed the PSG nickel gettering effect of the SMIC poly-Si at the same time.

III. SMIC Poly-Si Devices

A. Device Fabrication

The device fabrication process is shown in Fig. 4. Details of the process are as follows. First a 500-nm thermal oxide was grown on 4-in c-Si wafers as the starting substrate. A 50-nm a-Si active layer was deposited by LPCVD at 550 °C. After immersing in the nickel nitrate solution, the samples were annealed at 590 °C for 4 hours which fully crystallized the a-Si films. By controlling the immersion time in the nickel nitrate solution, two different kinds of grain were obtained. Four samples, two with dish-like domains and two with wadding-like domains, were immersed in 37% HCl for 3 h to get rid of the remaining nickel on the poly-Si surface. Then one sample with dish-like domains and one sample with wadding-like domains were covered with 700nm PSG, and annealed at 590 °C for 4 hours for nickel gettering. The gas flow of PSG deposition is as follows: Silane: 24 sccm, Oxygen: 100 sccm, 50% Phosphine in Silane: 8 sccm. The PSG was then etched with 777 etchant at room temperature. Thus there are four types of samples: (a) Type-A with dish-like poly-Si domains with PSG gettering, (b) Type-B with dish-like poly-Si domains without PSG gettering' (c) Type-C with wadding-like poly-Si domains with PSG gettering, and (d) Type-D with wadding-like poly-Si domain without PSG gettering.

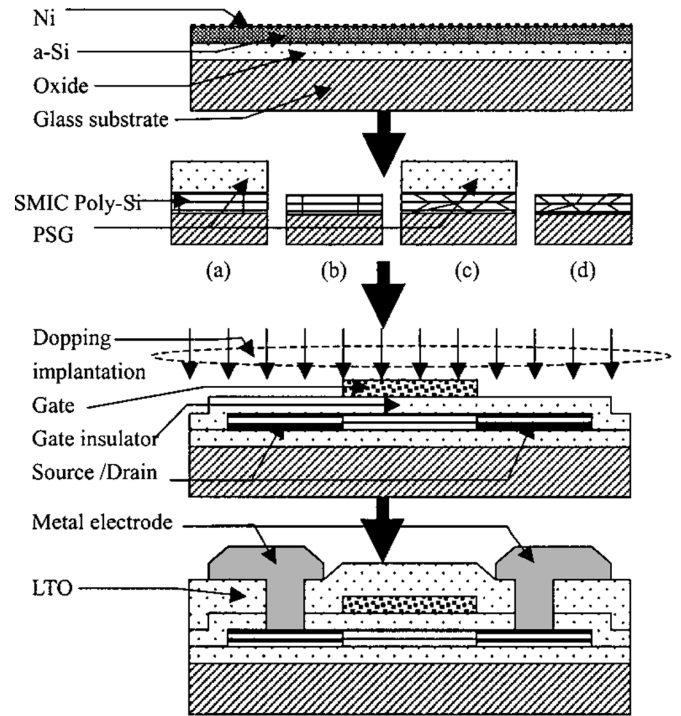

Fig. 4. Process flow for TFT fabrication.

These four kinds of poly-Si films were then patterned into active islands by wet etching with Freckle etchant. The freckle etchant is mainly composed of CH_3COOH, HBF_4, HNO_3 and H_3PO_4. Then the photoresist was removed by a solution of H_2SO_4 and H_2O_2 at 120 °C. 100-nm low temperature oxide (LTO) of was subsequently deposited by LPCVD at 425 °C as the gate insulator after the native oxide was removed by 1% HF. Following the deposition of 280-nm LPCVD poly-Si which was

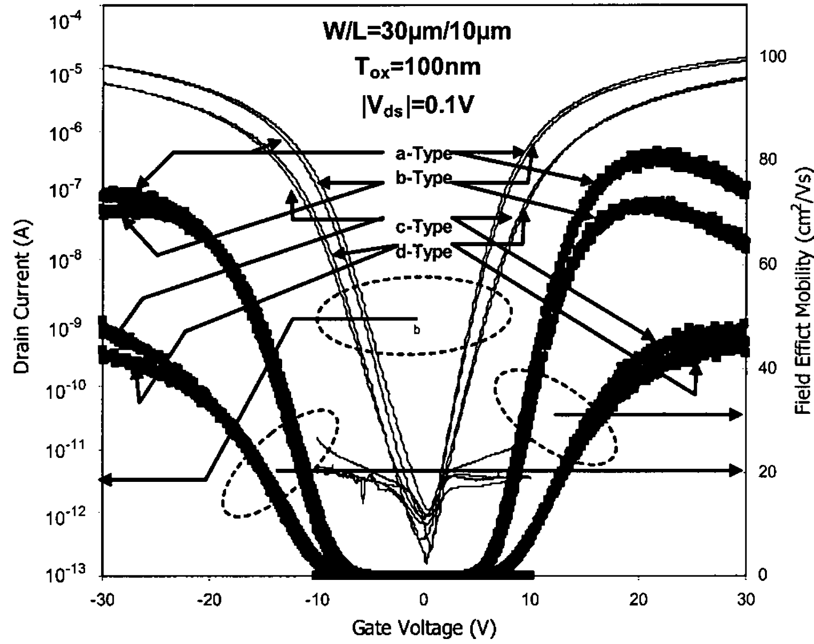

Fig. 5. Drain current and field-effect mobility versus gate voltage of n-and p-type SMIC-TFTs fabricated with of dish-like domain and wadding-like domain poly-Si, with and without PSG gettering.

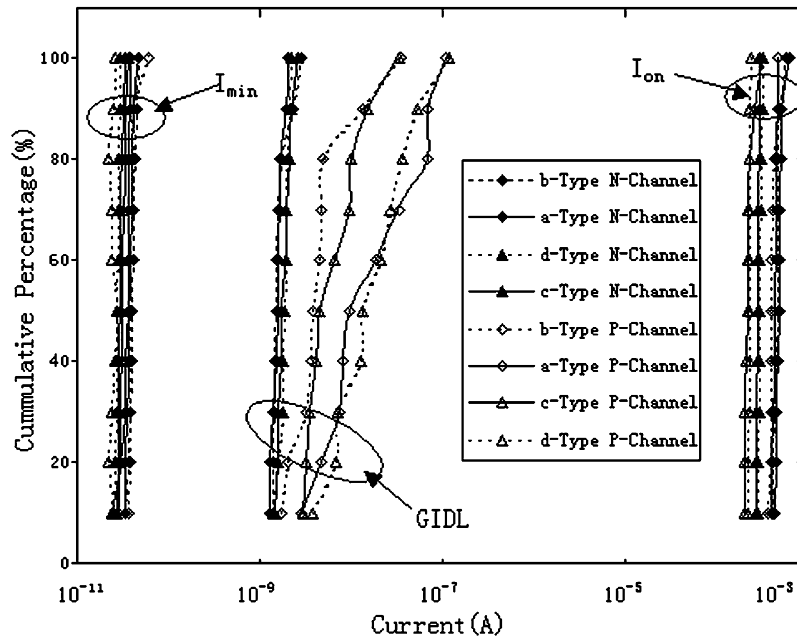

Fig. 6. Statistical distributions of the $I_{\rm on}$, $I_{\rm off}$, and GIDL of p- and n-type SMIC-poly-Si TFTs.

patterned into gate electrodes, phosphorus and boron at a dose of $4\times10^{15}/\text{cm}^2$ were implanted into the source, drain, and gate regions of n- and p-type TFTs, respectively. A 500-nm LTO isolation layer was deposited and the dopants were activated. Contact holes were opened before 500-nm aluminum-1%Si was subsequently sputtered and patterned as contacts. Contact sintering was then performed in forming gas at 420 °C for 30 min.

B. TFT Performance Measurement and Analysis

Electrical characteristics, uniformity and reliability of p-channel and n-channel TFTs using the four types of materials as the active layer were measured with HP4156 semiconductor parameter analyzer. Firstly, transfer characteristic curves for TFTs of which W/L were 30/10 with a 100-nm gate insulator layer were tested. The measurement conditions of p-type TFTs were as follows: $V_{\rm ds} = -0.1$ V and $V_{\rm ds} = -5$ V. For n-type TFTs they were: $V_{\rm ds} = 0.1$ V, and $V_{\rm ds} = 5$ V. The field effective mobility $(\mu_{\rm FE})$ and the linearly extrapolated threshold voltage $(V_{\rm th})$ were extracted using the following drain current (I_d) model equation in the quasi-linear regime of operation:

$$I_d \approx \frac{\mu C_{\rm ox} W}{L}(V_{\rm gs} - V_{\rm th})V_{\rm ds} \quad (1)$$

TABLE II
AVERAGE VALUE AND DISTRIBUTION OF SMIC TFT CHARACTERISTICS

		N-Channel				P-Channel			
		Type-A	Type-B	Type-C	Type-D	Type-A	Type-B	Type-C	Type-D
I_{on} $\|V_{ds}\|$=5V $\|V_{gs}\|$=30V	Average (10^{-4} A)	5.1	4.8	3.0	3.2	4.6	4.3	2.4	2.4
	Deviation (%)	11.1	9.7	3.4	3.8	5.8	7.9	16.3	2.3
I_{off} Minimum $\|V_{ds}\|$=5V	Average (10^{-11} A)	3.7	4.1	3.0	1.9	3.7	4.1	3.1	2.5
	Deviation (%)	4.8	9.5	6.4	13.3	14.9	17.5	10.3	6.9
I_{off} $\|V_{ds}\|$=5V $\|V_{gs}\|$=10V	Average (10^{-9} A)	1.6	1.8	1.9	2.8	33.1	7.83	9.52	30.3
	Deviation (%)	16.2	26.9	18.7	5.1	108.5	130.3	101.6	113.5

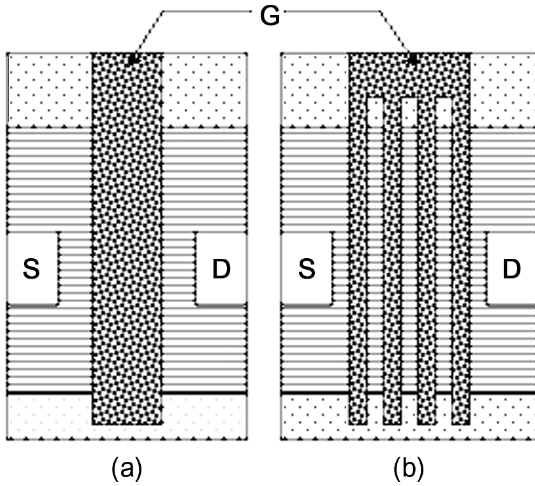

Fig. 7. Layout of single- and multi-gate TFT.

where V_{gs}, V_{th}, and V_{ds},are the gate bias, threshold voltage, and voltage between drain and source, respectively, C_{ox} is the gate insulator capacitance per unit area, W and L are the effective channel width and length of TFT. The field-effect mobility (μ_{FE}) at low drain voltage is given by

$$\mu_{\mathrm{FE}} = \frac{Lg_m}{WC_{\mathrm{ox}}V_{\mathrm{ds}}} \tag{2}$$

where g_m is the transconductance. The reported field-effect mobility is the maximum value measured.

Fig. 5 shows the transfer characteristics of SMIC poly-Si TFTs and their field-effect mobility. The transfer characteristics curves show that both p-channel and n-channel TFTs fabricated on dish-like domains have a much better performance than that fabricated on wadding-like domains. They exhibit smaller threshold voltage, lower subthreshold swing and higher drain current. The same curves also show that PSG gettering has little effect on the transfer characteristics at low drain voltage. However, the transfer characteristics curves of TFTs with PSG gettering shift to the left by 0.3–0.5 V from those of TFTs without. The shift is probably due to the decrease of nickel or the doping effect of phosphorus from PSG.

The n-channel TFTs with dish-like domain poly-Si exhibit a maximum field effect mobility of $70 \sim 80\ \mathrm{cm^2/V \cdot s}$ at about 20 V. The μ_{FE} of TFTs with PSG gettering are about $5 \sim 10\ \mathrm{cm^2/V \cdot s}$ higher than that without PSG gettering. For n-channel TFTs using wadding-like domains, the field-effect mobility are about $45 \sim 50\ \mathrm{cm^2/V \cdot s}$, with a maximum at 30 V. TFTs with PSG gettering exhibit a field effect mobility of $50\ \mathrm{cm^2/V{\cdot}s}$, which was $3 \sim 5\ \mathrm{cm^2/V{\cdot}s}$ higher than that without PSG gettering. As to p-channel TFTs using dish-like domains as active layer, the field effect mobility is about $70 \sim 75\ \mathrm{cm^2/V{\cdot}s}$, with a maximum at -25 V. Additionally, the p-channel TFTs with PSG gettering exhibited $5\ \mathrm{cm^2/V \cdot s}$ higher mobility than the TFTs without PSG gettering. The field effect mobilities of p-channel TFTs with wadding-like domain are in the average of $40 \sim 50\ \mathrm{cm^2/V \cdot s}$. Again TFTs with PSG gettering show $3 \sim 5\ \mathrm{cm^2/V \cdot s}$ higher mobilities than that without PSG, with the maximum occurring at about -30 V. Therefore, it can be seen that, the performance of SMIC poly-Si TFTs is mainly determined by the domain structure of the poly-Si films, and show only a little improvement with PSG gettering. Table I shows the electrical parameters of these eight kinds of SMIC-poly-Si TFTs, measured at $|\mathrm{V_{ds}}| = 0.1$ V and $|\mathrm{V_{ds}}| = 5$ V.

Table I also shows the ratio of on-state to off-state currents. Both the ratio of I_{on} to I_{min} (the minimum value of I_d) and the ratio of I_{on} to I_d-10 V ($\mathrm{V_{gs}} = -10$ V for n-type TFTs, $\mathrm{V_{gs}} = 10$ V for p-type TFTs) were investigated. The latter mainly indicated the effect of GIDL. From the table, it can be seen that, when $|\mathrm{V_{ds}}| = 5$ V, $I_{\mathrm{on}}/I_{\mathrm{min}}$ of all dish-like domain poly-Si TFTs exceed 10^7, and those of wadding-like domain poly-Si TFTs are close to 10^7. But for p-channel TFTs, when $\mathrm{V_{gs}} = 10$ V, I_d dramatically increases by as much as 500 times.

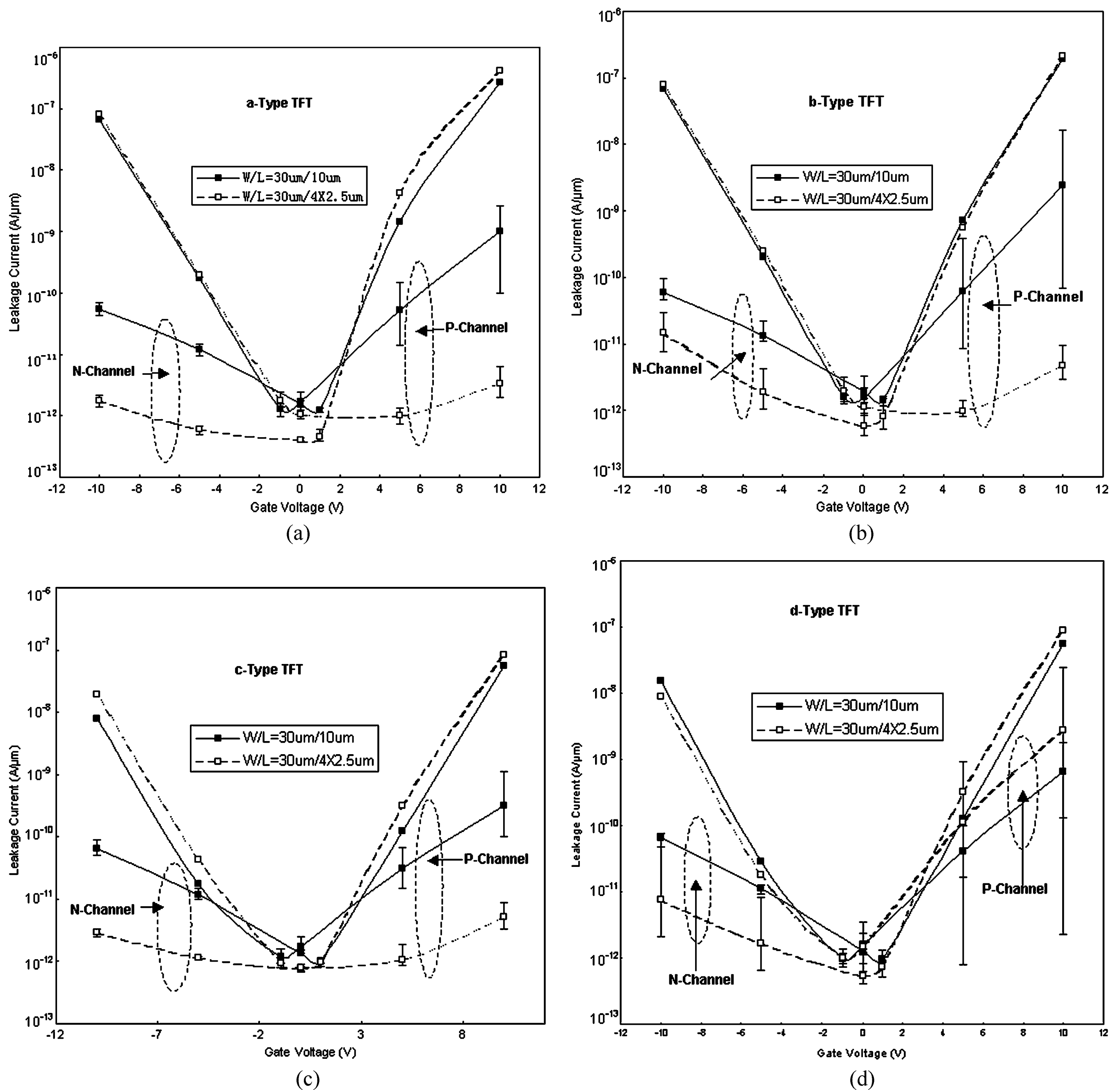

Fig. 8. Leakage current of n- and p-type SMIC-TFTs fabricated with: (a) dish-like domain with PSG gettering; (b) dish-like domain without PSG gettering; (c) wadding-like domain with PSG gettering; and (d) wadding-like domain with PSG gettering.

This is an indication of serious GIDL effect. Obviously they do not meet the requirements for making an active matrix device since $_{\mathrm{on}}/I_{\min}$ is now less than 10^5.

The uniformity of the SMIC poly-Si TFTs was also studied. 20 TFTs with the same device structure distributed over the 4-in wafer were sampled. The same device parameters were extracted to be analyzed and compared. The TFTs had $W/L = 30\ \mu\mathrm{m}/10\ \mu\mathrm{m}$, and 100-nm LTO as gate isolation layer and were tested under the measurement condition of $V_{\mathrm{ds}} = 5$ V and $V_{\mathrm{ds}} = -5$ V for n-channel and p-channel TFTs, respectively. I_{on} ($V_{\mathrm{gs}} = -30$ V for p-channel TFTs and $V_{\mathrm{gs}} = 30$ V for n-channel TFTs), $I_{\min}$, and GIDL ($V_{\mathrm{gs}} = 10$ V for p-channel TFTs and $V_{\mathrm{gs}} = -10$ V for n-channel TFTs) were compared. As shown in Fig. 6, the I_{on}, $I_{\min}$ of both p- and n-type TFTs and GIDL of n-type TFTs are tightly distributed, which indicates good uniformity of n-type TFTs. However, the distribution of GIDL of p-type TFTs remains quite broad across all devices measured.

One can see that relative scattering (defined as standard deviation divided by the average) of the I_{on} of wadding-like domain TFTs ($\sim$2%–3%) is lower than that of dish-like domain TFTs ($\sim$3%–5%). However, the distributions of I_{on} of both n-type and p-type TFTs are basically the same. As to the distribution of the $I_{\min}$ (minimum leakage current), the relative scattering of the p-channel and n-channel TFTs of wadding-like domain is close to 7%$\sim$15%. However, the relative scattering of dish-like do-

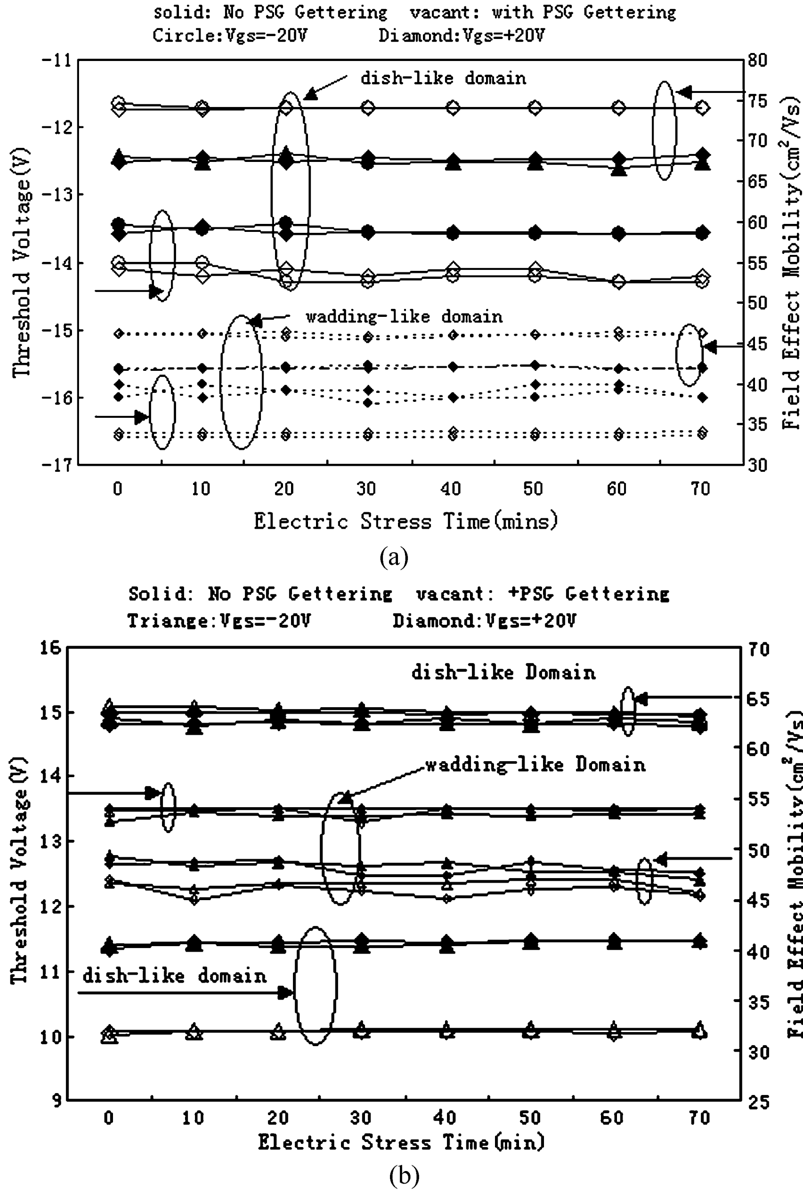

Fig. 9. Positive and negative gate bias stress (at $V = \pm 20$ V) effects on the field-effect mobility and the threshold voltage shift for (a) p-channel and (b) n-channel SMIC TFT.

main p-channelTFTs is about 15%∼20%, which is much higher than that of n-channel TFTs, of 5%∼10%.

The scattering of GIDL is markedly higher than $I_{\rm on}$ and $I_{\rm min}$ above mentioned. The relative scattering degree of n-channel TFTs and p-channelTFTs, wadding-like domain or dish-like domain, are 6%∼30% and 100%∼150%, respectively. The average parameter and relative scattering are listed in Table II.

To overcome the issue of leakage, a multi-gate structure (Fig. 7) was investigated. Indeed it was found that this structure significantly decreased the leakage current and the relative scattering of all eight kinds of SMIC poly-Si TFTs. Fig. 8 shows the results comparing the leakage currents and GIDL between the four-gate and single gate TFT. The multi-gate TFTs have a ratio of channel width and length of 30 μm/4 $\times$ 2.5 μm and the single gate TFTs have a ratio of 30 μm/10 μm. They were measured under the same condition of $|V_{\rm ds}| = 5$ V, $V_{\rm gs} = -5$ V (for n-channel) and $V_{\rm gs} = 5$ V (for p-channel). Fig. 8(a) and (b) shows the leakage current as a function of $V_{\rm gs}$ of the TFTs using dish-like domain SMIC poly-Si as active layer with PSG gettering and without PSG gettering, respectively. The relationship between leakage current and $V_{\rm gs}$ of the TFTs with wadding-like domain SMIC poly-Si with and without PSG gettering are shown in Fig. 8(c) and Fig. 8(d).

From Fig. 8 we can see that, excluding wadding-like domain SMIC poly-Si TFTs without PSG gettering, the lowest current density of n- and p-channelTFTs fell down to 10^{-12} A/μm owing to the multi-gate structure. The GIDL of n-channel TFTs with a four-gate structure decreased by 1.5 magnitude orders than single-gate TFTs at $V_{\rm gs} = -10$ V. Meanwhile, compared to p-channel single-gate TFTs, the GIDL of four-gate TFTs was dropped nearly 2.5 magnitude orders when $V_{\rm gs} = 10$ V. Just the wadding-like domain poly-Si TFTs without PSG gettering has no improvement on the leakage current after using the multi-gate structure, still showing large leakage current and high scatter degree. This may indicate that the wadding-like domain poly-Si without PSG gettering had a higher grain boundary

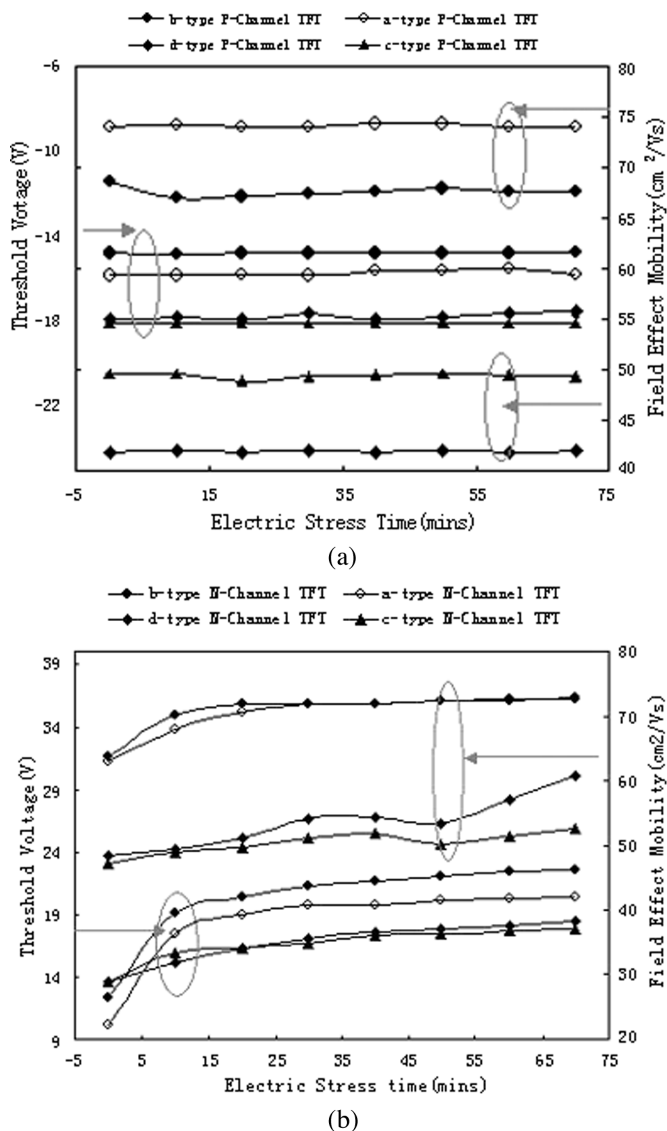

Fig. 10. Hot-carrier bias stress effect on the field-effect mobility variation and the threshold voltage shift for the SMIC TFT versus bias stress time.

defect density and more nickel remained, which can easily induce large leakage current. So even employing 4-gate structure, the leakage currents are still not satisfactory.

Fig. 9 shows the reliability of eight kinds TFTs (p/n channel) with four kinds of poly-Si as active layer under the gate bias-stress. The low voltage transfer characteristic curves of TFTs with $W/L = 30\ \mu\text{m}/10\ \mu\text{m}$, $T_{\text{ox}} = 100\ \mu\text{m}$ were measured every 10 min with the gate stress at $\text{V}_d = \text{V}_s = 0$ V, $\text{V}_{\text{gs}} = \pm 20$ V. The field-effect mobility and threshold voltage were abstracted and compared. As shown in Fig. 9(a) and (b), no change in the threshold voltage and field-effect mobility for both n-channel and p-channel SMIC poly-Si TFTs was found under the effect of gate stress mentioned above for over an hour. It can be said that SMIC poly-Si TFTs exhibit excellent reliability under gate stress.

Fig. 10 shows the reliability of above 8 kinds of TFTs under a hot-carrier bias-stress. The measurement conditions were $\text{V}_{\text{gs}} = -25$ V, $\text{V}_{\text{ds}} = -20$ V for p-channel TFTs and $\text{V}_{\text{gs}} = 10$ V, $\text{V}_{\text{ds}} = 20$ V for n-channel TFTs. The threshold voltage and field-effect mobility were abstracted from the low voltage transfer characteristic curves of TFTs with $W/L = 30\ \mu\text{m}/10\ \mu\text{m}$, $T_{\text{ox}} = 100$ nm measured every 10 min. As shown in Fig. 10(a), the four kinds of p-channel poly-Si TFTs, dish-like domain with PSG gettering, dish-like domain without PSG gettering, wadding-like domain with PSG gettering and wadding-like domain without PSG gettering, possess excellent reliability, without any change in threshold voltage and field effect mobility. However, as shown in Fig. 10(b), under the hot-carrier bias-stress, the threshold voltage and field effect mobility of n-channel TFTs using all the four kinds poly-Si as active layer are markedly changed, especially in the first 20 min. The threshold voltage of dish-like domain TFTs with PSG gettering increased from 12 V original and to 21 V at the first 20 min of hot-carrier bias-stress time and from 10 to 18 V of TFTs without PSG gettering. In the subsequently stress time, it continued to increase slowly. The field mobility also demonstrates similar tendency, increasing fast at the beginning and then slowly. The shifts in the threshold voltage of n-channel wadding-like domain TFTs as a function of hot-carrier bias-stress time was smaller than that of n-channel dish-like domain TFTs, just 2 V at the first 20 min. The TFTs without PSG gettering had larger shift than the TFTs with PSG gettering. But if the tress time is longer than 20 min, these kinds of TFTs had the accordant trend.

IV. Conclusion

In this paper, we have demonstrated the new technique of forming LTPS by a solution process. The technique has the advantage of ease of processing and reliable control of the Ni content in the MIC process. It was found that by controlling the dipping time, which essentially controls the amount of Ni adsorbed on the a-Si surface, different domains can be obtained. The dish-like domains and wadding-like domains have rather different structural and electrical properties. The Hall mobilities of dish-like domain poly-Si are $46.5\ \text{cm}^2/\text{V} \cdot \text{s}$ for n-type and $30.8\ \text{cm}^2/\text{V} \cdot \text{s}$ for p-type. These values are obviously higher than that of wadding-like domains, being $25.2\ \text{cm}^2/\text{V} \cdot \text{s}$ for n-type and $22.5\ \text{cm}^2/\text{V} \cdot \text{s}$ for p-type.

TFTs were fabricated using these two kinds of poly-Si films as the active layer and employing the PSG gettering technology. The TFTs on dish-like domain exhibit a typical field effect mobility of $70 \sim 80\ \text{cm}^2/\text{V} \cdot \text{s}$, while it is $40 \sim 50\ \text{cm}^2/\text{V} \cdot \text{s}$ for wadding-like domain TFTs. The performance can be improved somewhat with PSG gettering. With a multi-gate structure, leakage current of n/p-channel SMIC poly-Si TFTs can be reduced down to $10^{-12}\ \text{A}/\mu\text{m}$ or even lower, the GIDL and the distribution uniformity of leakage current can also be markedly improved.

The p-channel SMIC poly-Si TFTs had very stable performance against gate bias stress as well as hot-carrier bias stress. Therefore, with the dish-like domain poly-Si film as active layer, employing PSG gettering technology, and a multi-gate structure, both n- and p-channel TFTs can have excellent electrical performance, good uniformity and high reliability. SMIC is a promising technology to realize the low cost, simple process poly-Si circuit for flat-panel displays.

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