Passively addressed FLC display possessing an inherent gray scale and memory

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Abstract — A passively addressed 64 × 64 ferroelectric liquid-crystal display (FLCD) has been developed. The display matrix has a 33 × 33 mm^2 aperture, and the FLC layer thickness is 5.2 ± 0.2 μm. The display device operates with a frame frequency of 30 Hz (at V_{row} = ±18 V, V_{col} = ±9 V, T = 23°C), generating a continuous gray scale which can be memorized for more than 10 days after the driving voltage is switched off. A new approach for multiplex electronic addressing of the FLCD gray scale is proposed. The conditions of the hysteresis-free gray-scale generation for multiplex addressing and the gray-scale memorization after the voltage is switched off, as well as the time steadiness of memorized images, are considered.

Keywords — *FLC display, gray scale, memory, multistability.*

1 Introduction

The inherent physical gray scale of passively addressed FLCDs can be obtained only if the FLC possesses high spontaneous polarization P_s > 50 nC/cm^2.[1,2] Then, ferroelectric domains exist, being one of several possible reasons for gray scale. Generally, any type of spatial nonuniformity of helix-free FLCs[3] coupled with minimization of the FLC free energy can be considered principally as a base for the gray scale. On the contrary, at high P_s, depolarizing fields appear in FLC cells, suppressing the bistability if the aligning layers are thick enough.[4] Therefore, extremely thin aligning layers are necessary for the development of a passively addressed FLCD having gray scale. One of the aligning layers can be removed, providing the best quality for the FLC layer photoalignment,[5] but such an asymmetry of the boundary conditions provides asymmetry of the energy of the FLC anchoring with boundaries. This can create problems with the steadiness of the bistability that is a necessary condition of multiplex addressing. Therefore, all these problems will be considered in our work. A principle of multiplex electronic addressing of FLCDs with the gray scale at a fixed frame time will also be discussed.

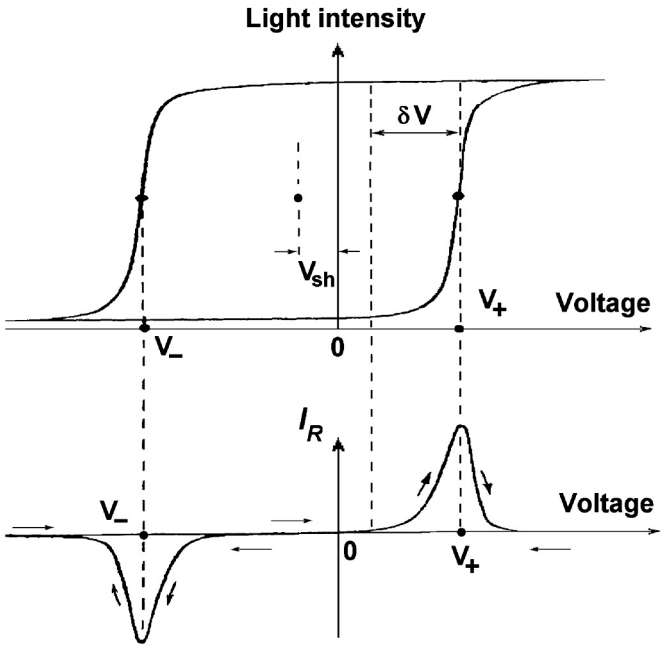

FIGURE 1 — Top – a typical hysteresis loop for a 6-μm layer of an FLC-497-based cell exhibiting a shift in the hysteresis loop center at zero voltage; bottom – a typical polarization reversal current of the cell. The aligning layer thickness is 12 nm; the frequency is 0.02 Hz.

2 Samples and measurements

Asymmetric boundary conditions[5] were used for the modeling and manufacturing of an FLCD. For this approach, only one ITO surface of the FLC cells was covered with a photoaligning substance (azobenzene sulfuric dye SD-1 layer) and another one was simply washed in *N*,*N*-dimethylformamide (DMF) and covered with 5.2- or 6.0-μm calibrated spacers. The azo-dye solution was spin-coated onto an ITO electrode and dried at 155°C. A polarized UV light beam was formed by using a super-high-pressure Hg lamp, an interference filter at 365 nm, and a polarizing filter. Light with an intensity of 6 mW/cm^2 and a wavelength of 365 nm was irradiated normally onto SD-1 layers. The FLC composition FLC-497 (on specification of P. N. Lebedev Physical Institute of the Russian Academy of Sciences) was injected into the cells in an isotropic phase by capillary action at T = 85°C. This FLC composition possesses a spontaneous polarization P_s = 95 nC/cm^2 and a tilt angle θ = 27°

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at $T = 23°C$. The phase transition sequence is as follows: Cr $\rightarrow^{4°C}$ C* $\rightarrow^{57°C}$ A* $\rightarrow^{76°C}$ Is. The helix pitch of the FLC tends to infinity in all the bulk due to compensation by two chiral dopants with the same signs as the spontaneous polarization, but opposite signs of their handedness.[3]

Electro-optical measurements were carried out using an ordinary electro-optical set-up based on a He–Ne laser, a Hewlett-Packard Infinum oscilloscope, and a rotating table for adjusting the angular position of FLC cells placed between crossed polarizers. A programmed generator was used for experimental simulations of the multiplex operation.

Measurements of the anchoring energy of the FLC with aligning surfaces were carried out according to a method proposed in Ref. 6. The idea is based on measurements of static hysteresis loops of FLC cells. "Static" means the frequency interval 10^{-3}–10^{-2} Hz, where there is no dependence of the voltage coercivity V_c on the applied voltage frequency.

The voltage coercivity can be defined according to Fig. 1 as

$$V_c = V_+ - V_-, \tag{1}$$

where V_+ and V_- are the switching voltage thresholds at corresponding positive and negative voltage.[6]

A shift V_{sh} in the center of the hysteresis loop at zero voltage, which usually takes place in FLC cells, can be evaluated according to Fig. 1 as

$$V_{sh} = (V_+ - V_-)/2. \tag{2}$$

This is a very important point in our analyses of the bistability steadiness because if

$$V_{sh} \geq V_c/2, \tag{3}$$

then the bistability evidently does not exist (Fig. 1).

3 Criteria of bistable FLC switching

To evaluate the bistability steadiness of display cells, both in static and dynamic cases, we propose a new criterion:

$$S_b = (^1/_2\, V_c - |V_{sh}|)/\delta V. \tag{4}$$

The parameter δV in Eq. (4) indicates a region inside the hysteresis loop where the light intensity at the output of FLC cell depends on the applied-voltage magnitude or the polarization reversal current is also nonzero (Fig. 1, bottom). Generally, one can evaluate the bistability steadiness even without any electro-optical measurements of the hysteresis loops simply by measuring the polarization reversal current diagrams (compare the top and bottom curves of Fig. 1). The perfect bistability both for the static and dynamic cases takes place, if $S_b \geq 1$, because under this condition both the dark and bright saturation levels of the light transmission obtained at applied voltage $V > V_+$ and $V < V_-$ can be memorized at zero voltage (when the voltage is switched off and the cell electrodes are shorted) without any change (Fig. 1). If $S_b < 0$, then the hysteresis loop is completely located in positive or negative region of the voltage, and perfect monostable operation of a display cell occurs. Such a cell can memorize only one fixed light transmission level after the voltage is switched off, and this case is completely inappropriate for passive multiplex addressing of displays. An intermediate region of S_b magnitudes – $0 \leq S_b < 1$ – corresponds to continuous transition from perfect bistability to perfect monostability of the display cells.

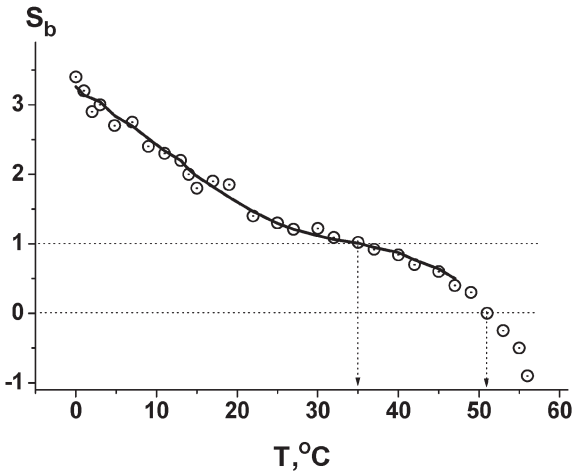


FIGURE 2 — Temperature dependence of the bistability parameter S_b measured for a 6-μm FLC-497-based cell with asymmetric boundary conditions. The SD-1 layer thickness is 9 nm, the frequency of the triangular voltage $f = 0.005$ Hz, the voltage amplitude is ±3.0 V.

The steady bistability with $S_b \geq 1$ for the static case (unlimited memory time) does not exist within the entire temperature region of smectic-C* phase of the FLC because of the strong temperature T dependence of $S_b(T)$. For example, in a 6-μm cell with FLC-497 and asymmetric boundary conditions manifests the temperature region with $S_b \geq 1$ at $T \leq 35°C$, but at $51°C \leq T \leq 56°C$ the perfect mono-stability takes place because $S_b \leq 0$ (Fig. 2). Evaluation of the temperature dependence of the bistability steadiness according to the criterion S_b have been confirmed by direct observations of bistable and mono-stable electro-optical responses in the corresponding temperature regions.

4 Optical manifestations and probable origin of ferroelectric domain modulation by the electrical field

The FLC gray scale arises from the so-called ferroelectric domains that appear in a cell due to FLC high spontaneous polarization[1,2] (Fig. 3). The electrically controlled structure of ferroelectric domains (observed between two crossed polarizers) is spatially modulated, *i.e.*, characterized by a regular structure of black-and-white stripes along the FLC smectic planes with the period, which is almost equal to the ferroelectric domain period [compare Figs. 3(a) and 3(b)]. Bright stripes indicate spatial regions where the FLC director is completely switched and memorized, while black stripes correspond to absolutely nonswitched regions.

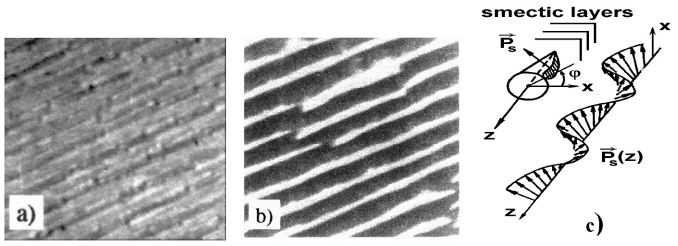


FIGURE 3 — (a) a 40 × 40-μm-sized microphotograph of a typical texture of ferroelectric domains before the driving-voltage application (5.2-μm FLC-497-based cell with asymmetric boundary conditions, SD-1 layer thickness is 9 nm); (b) the same area as the FLC cell in Fig. 3(a) but the texture is memorized after application of the sequence of driving-voltage pulses; (c) a model of the spatial modulation of the spontaneous polarization vector due to ferroelectric domains[7] (*x* axis is perpendicular and *z* is parallel to the solid substrates of the cell).

Sharp boundaries occur between the black and white regions illustrating the fact that the FLC director possesses only two steady positions. This means that each smectic layer manifests true bistability without memorizing any intermediate states between "black" and "white" states. The apparent light transmission of the structure shown in Fig. 3(b) is a result of a spatial averaging of "black" and "white" areas over the light aperture, which is much larger than the structure period. The gray scale appears as a result of this averaging; therefore, multistability of only light-transmission levels takes place. Memorization of all generated gray-scale levels for unlimited time is possible and was confirmed in our experiments.

5 FLCD addressing

5.1 Multiplexing scheme

Possible driving voltage shapes that provide the gray scale in passively addressed FLCDs have been developed by taking

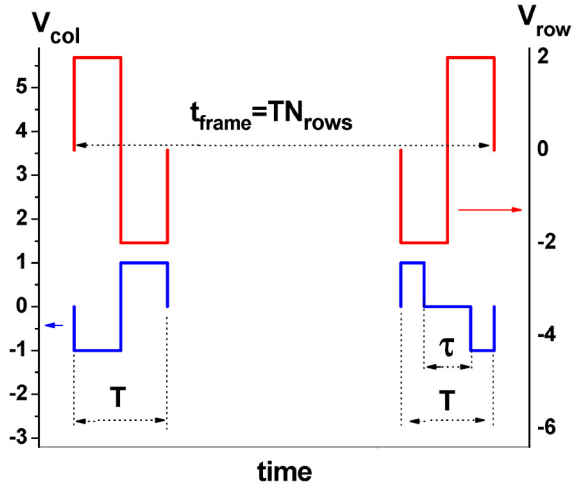


FIGURE 4 — Illustration of the gray-level passive-addressing scheme for FLC displays. At $\tau/T = 0$ (the column pulse in left bottom corner), the binary mode takes place. The relative intensity of gray levels depends on the τ/T parameter if $0 < \tau/T < 1$ (the column pulse in right bottom corner).

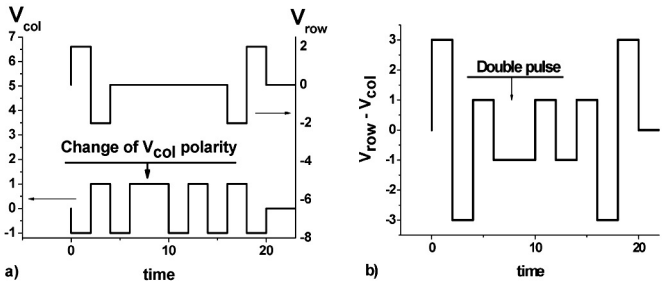


FIGURE 5 — A binary multiplexing voltage applied according to the Seiko standard to any pixel of an 4 × 4 FLC matrix during the frame time: (a) row voltage – top, column voltage – bottom; (b) the voltage between a row and a column applied to the FLC layer.

into account two basic ideas. These are the well-known Seiko-standard multiplexing scheme,[8] which provides a binary multiplexing mode of passively addressed FLC displays, and the pulse-width-modulation (PWM) principle which provides, for instance, the gray scale of STN displays.[9] Proposed modification of the Seiko-standard multiplexing scheme relates to the column voltage shape and polarity only while the row voltage shape is the same as for the classic Seiko standard. Instead of pair "negative-positive" row voltage pulses, the modified pair is of the same total duration T that equals the row addressing time that should be generated (Fig. 4). Only time interval τ (Fig. 4) can be changed, and the polarity of the pulses can be reversed. A PWM rate can be defined as τ/T.

Let us consider, for instance, the voltage applied to any pixel of an 4 × 4 FLC matrix at binary multiplex operation according to the Seiko-standard multiplexing scheme (Fig. 5). It contains a double crosstalking pulse [Fig. 2(b)] that appears because a change in column voltage polarity is necessary to switch any pixel according to the basic idea (Fig. 4). On the other hand, the double pulse provides intensive crosstalking pulse in the cell electro-optical response of the FLC. One of goals of our approach is the suppression of the mentioned double pulse. It can be performed by using the pulse width modulation (PWM) method also. To suppress the double pulse, the column voltage polarity change should be realized by the modulated pulse at fixed rate τ/T = 0.5. The result is shown in Fig. 6.

The main goal of our approach is to model the multiplexing voltage for gray-scale generation, taking into account the PWM method, and to suppress the double pulse shown in Fig. 5. This is possible to do by simply applying a PWM column pulse, which is shown in Fig. 4, to a selected column (Fig. 7). The row voltage is still the same as shown in Fig. 5(a). The column voltage applied to any pixel of the 4 × 4 FLC matrix during the frame time consists of three types of pulses which are important for gray-scale generation. These are pulses "1," "2," and "3" shown in Fig. 7 (bottom). Pulse "2" of the column-voltage polarity change is the pulse with a fixed rate τ/T = 0.5, the same as discussed above for the binary multiplexing voltage (Fig. 6). Pulses "1" and "3" are PWM pulses possessing polarities opposite to each other polarity with variable $0 \le \tau/T \le 1$ magnitudes. Just a

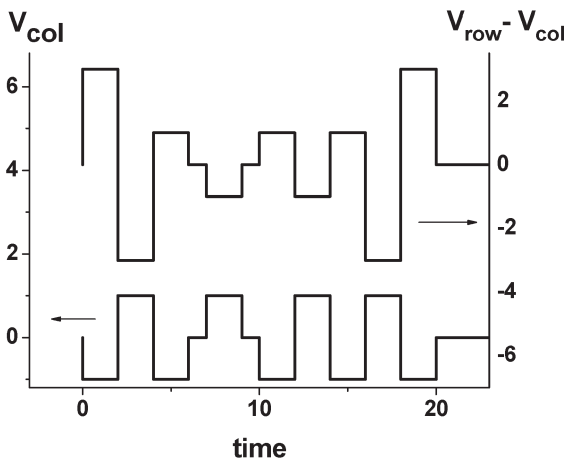


FIGURE 6 — A binary multiplexing voltage applied to any pixel of the 4 × 4 FLC matrix during the frame time: bottom – column voltage polarity change occurs simultaneously with the pulse width modulation; top – the voltage between a row and a column that applied to FLC layer.

sequence of pulses "1," "2," and "3" provides the generation of any gray-scale level of passively addressed FLCDs, if a variation of $0 \le \tau/T \le 1$ is realized. Additionally, the voltage $V_{row} - V_{col}$ (top diagrams in Figs. 6 and 7) during the frame time T_{frame} should satisfy the condition

$$\int_0^{T_{frame}} \left[V_{row}(t) - V_{col}(t) \right] dt = 0 \qquad (5)$$

to avoid any bias voltage, which suppresses both the binary and gray-scale modes in the FLC matrix.

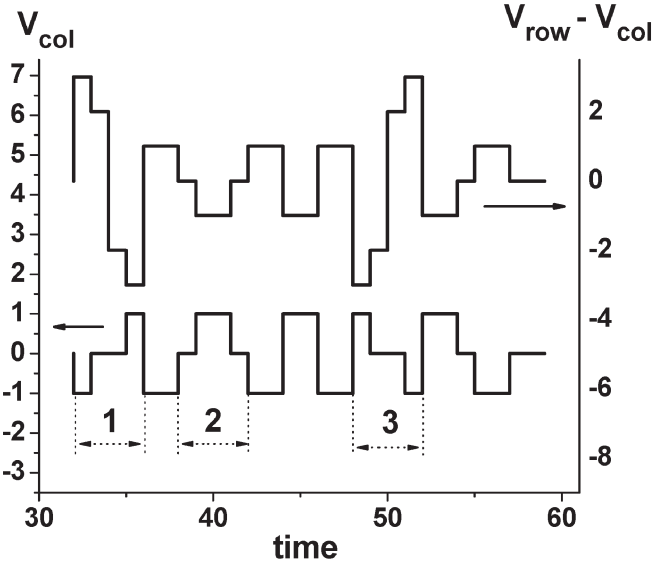


FIGURE 7 — Epures of gray-scale multiplexing voltage applied to any pixel of the 4 × 4 FLC matrix during the frame time: bottom – column voltage; top – voltage between a row and a column applied to the FLC layer. Pulses 1 and 3 of the column voltage are PWM pulses with variable $0 \le \tau/T \le 1$ magnitude, pulse 2 is the column-voltage polarity change pulse with fixed magnitude $\tau/T = 0.5$.

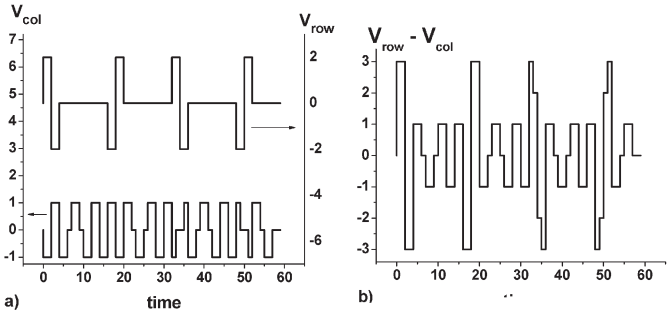


FIGURE 8 — Epures of multiplexing voltage applied to any pixel of the 4 × 4 FLC matrix during the frame time for addressing in sequential frames black, white, and any gray level: (a) bottom – column voltage; top – column voltage, (b) the voltage between a row and a column applied to the FLC layer.

Finally, in sequential frames the voltage for addressing black, white, and any of the gray levels in any pixels in the 4 × 4 FLC matrix looks like that shown in Fig. 8. The selection of gray-scale levels can be realized by waveforms shown in Fig. 8 by changing the τ/T magnitudes of selecting column pulses only. Let us repeat that the column-voltage polarity change must be at a fixed rate $\tau/T = 0.5$ for the addressing of all levels of light transmission: black, white, and any of gray levels.

5.2 Experimental simulation of gray-scale generation

A simulator of the multiplex voltage was used to generate the waveform shown in Fig. 8(b). This voltage was applied to an ordinary photoaligned FLC cell to simulate the electro-optical response of the pixels of the 4 × 4 FLC matrix

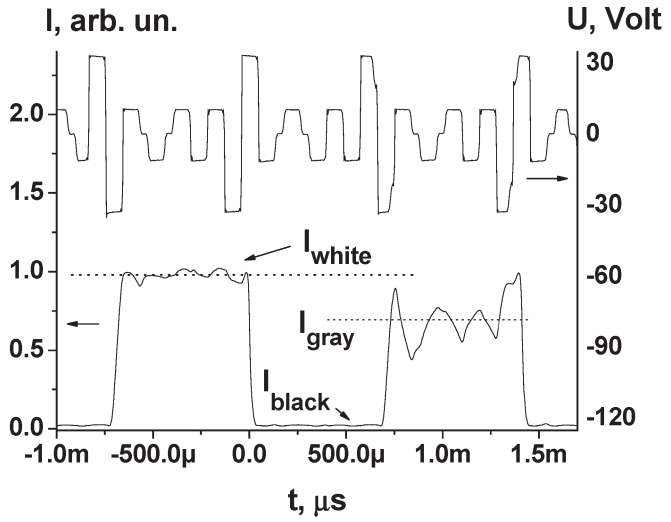


FIGURE 9 — Experimental simulation of white, black, and gray level addressing one of the pixels of the 4 × 4 FLC matrix in three sequential frames: top – the voltage between a row and a column applied to the FLC layer with $\tau/T = 0$ for black and white levels and $\tau/T = 0.25$ for gray levels; bottom – the electro-optical response of 6-μm FLC-497A-based photoaligned cell at $T = 22°C$.

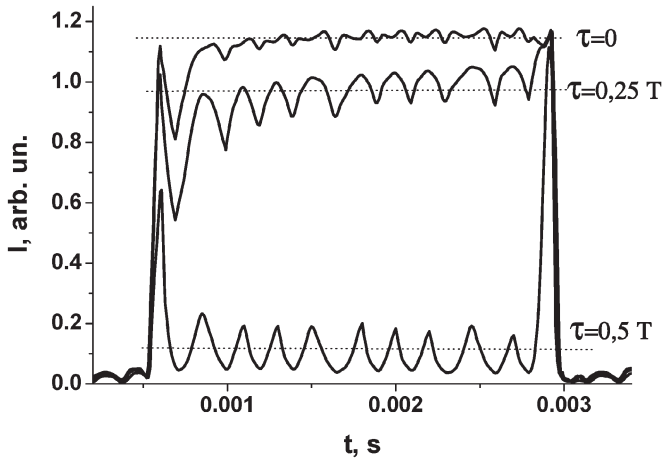


FIGURE 10 — The light transmission experimentally simulated for a 10 × 10 FLC matrix at the same frame for the fixed row but for three different columns, dependent on the magnitude of the τ/T ratio corresponding to these columns: top – $\tau = 0$; in the middle – $\tau = 0.25T$ (gray state); bottom – $\tau = 0.5T$ (gray scale).

(Fig. 9). One can see three levels of light transmission: I_{white}, I_{black}, and I_{gray}.

Let us now consider variations in the light transmission simulated experimentally for the case of a 10 × 10 FLC matrix, at the same frame for a fixed row but three different columns, dependently on the τ/T ratio magnitude corresponding to these columns (Fig. 8). The most important time interval for the gray-scale generation can be defined as

$$0.25 < \tau/T < 0.5, \tag{6}$$

because at $\tau/T = 0.25$ $I_{GS-0.25} = 0.85I_b$ and at $\tau/T = 0.5$ $I_{GS-0.5} = 0.104I_b$ (here I_b is the intensity of the transmitted light at the binary multiplex mode (see top line in Fig. 10 to recognize I_b).

6 Hysteresis-free and steady gray scale for passively addressed FLC display

The best condition for FLC bistable switching is the symmetrical hysteresis loop with $|V_{sh}| \to 0$ and $\delta V \to 0$ according to Eq. (4), while the hysteresis-free gray scale of FLCDs also requires a certain relationship between these two values. The relationship can be found if we suggest that the "black" state is the basic one, so the threshold V_{thB} of the bright level addressing is not less than the saturation voltage V_{SD} of the dark-state addressing (Fig. 11):

$$V_{thB} \geq V_{SD}. \tag{7}$$

Condition (7) provides addressing of all the levels of the light transmission using the right branch of the hysteresis loop. The left branch of the hysteresis loop is of no importance when the driving voltage exceeds the V_{SD} value. In this case, the hysteresis-free FLC addressing of all light transmission levels (gray scale) can be obtained.

The voltages V_{thB} and V_{SD} can be expressed as (Fig. 11)

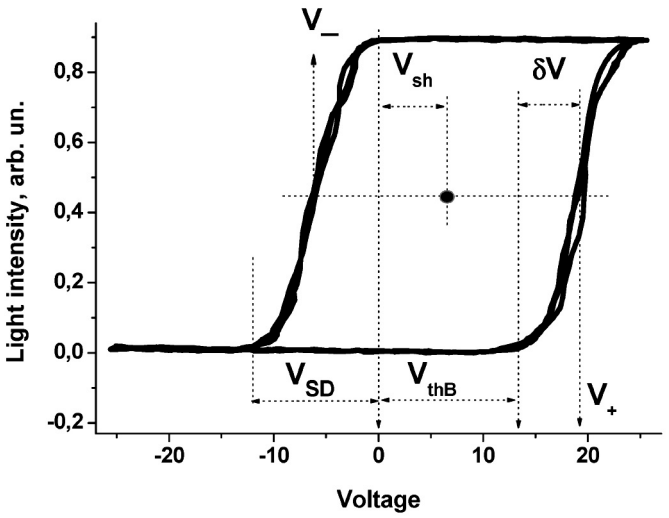


FIGURE 11 — The hysteresis loop of a 5.2-μm FLC-497-based asymmetric display cell. L_{SD-1} = 9 nm, the frequency of the triangular voltage f = 50 Hz, the amplitude is ±30 V, and T = 23°C. V_{thB} is the threshold voltage of bright-level addressing, and V_{SD} is the saturation voltage of the dark-state addressing.

$$V_{thB} = \frac{1}{2}V_c + |V_{sh}| - \delta V, \quad V_{SD} = \frac{1}{2}V_c - |V_{sh}| + \delta V, \tag{8}$$

and by combining (7) and (8), we get

$$|V_{sh}| \geq \delta V. \tag{9}$$

By taking into account Eqs. (4) and (9), we have necessary and sufficient conditions of the hysteresis-free gray-scale FLC addressing (Fig. 5):

$$\delta V \leq |V_{sh}| \leq \frac{1}{2}V_c - \delta V \tag{10}$$

or

$$1 \leq \frac{|V_{sh}|}{\delta V} \leq \frac{V_c}{2\delta V} - 1. \tag{11}$$

The addressing of gray-scale levels under conditions (10) and (11) is illustrated in Fig. 12 for the same FLC display cell and electric-field frequency f = 50 Hz, which was used for measuring of the loop shown in Fig. 11.

7 Inherent and controlled hysteresis loop shift: A role of the aligning surface polarity

As was shown above, the hysteresis-free and steady gray scale is possible under condition (11): the hysteresis loop must be asymmetrical relative to $V = 0$. In practice, a loop center is always shifted relative to $V = 0$ due to the different polarity of the boundary layers.

The polarity of ITO is quite different generally from the polarity of a SD-1 surface at asymmetric boundary conditions, as it is illustrated by a dependence of polar part of surface-free energy γ_S^P for a thickness of the SD-1 layer, which covers the ITO surface (Fig. 13). Besides, the γ_S^P

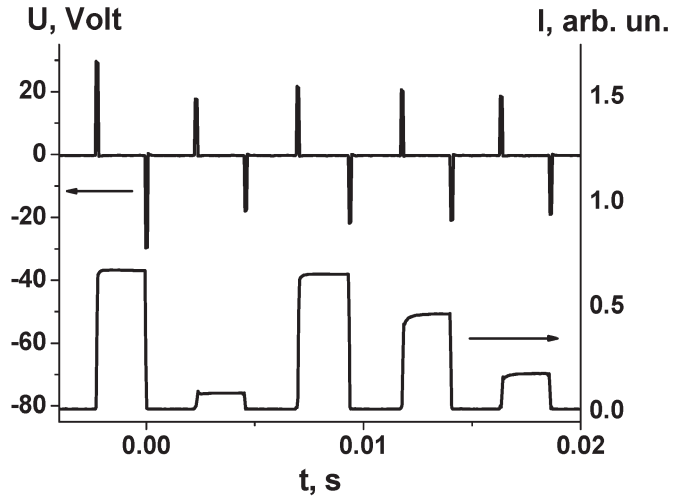


FIGURE 12 — Electrooptical response of 5.2-μm FLC-497-based asymmetric display cell. $L_{SD\text{-}1}$ = 9 nm, the frequency of the triangular voltage f = 50 Hz; the voltage amplitude varies from ±18 V to ±30 V, and T = 23°C. The relative intensity of the memorized gray levels in Fig. 12 exactly corresponds to the light-transmission levels selected from the right branch of the hysteresis loop shown in Fig. 11.

magnitude of the SD-1 surface, dependent on the SD-1 layer thickness, can be larger or smaller than the corresponding parameter of the pure ITO surface.

A difference ΔW_P of the polar segments of the energy of the FLC anchoring with boundaries can be expressed as[6]

$$\Delta W_P = P_s V_{sh}. \tag{12}$$

For the case of the asymmetric boundary conditions mentioned above, the $\gamma_S^P(L_{SD-1})$ dependence creates a strong difference ΔW_P in the polar segments of the FLC anchoring energy with boundaries: pure ITO and ITO covered with a SD-1 layer. Even the ΔW_P sign changes with changing aligning layer thickness (Fig. 14). Such a situation can be explained by taking into account the diagram shown in Fig. 13. According to Eq. (12), this means a considerable

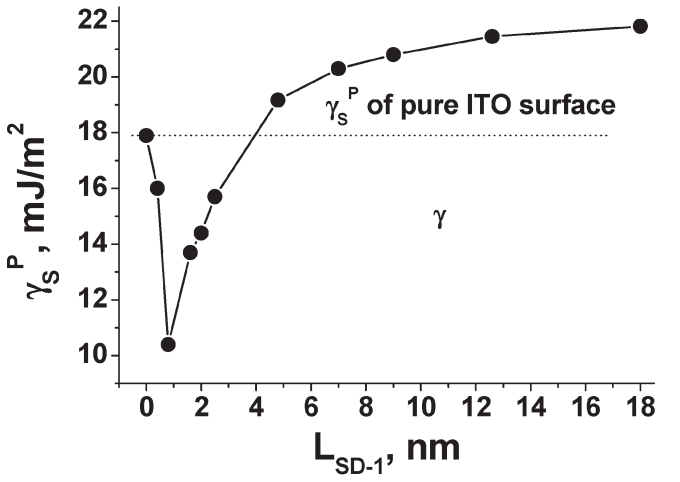


FIGURE 13 — Dependence of a polar segment of the surface-free energy of the photoaligning surface SD-1 covering the ITO surface on the SD-1 layer thickness.

and regular shift of the static hysteresis loops center with changing SD-1 layer thickness.

Another possible source of the hysteresis loop center shift is a depolarizing field[4,5] that exists in an FLC cell because of the contact of FLC with the aligning layers possessing different dielectric permittivity (in our case ε_{FLC} and ε_{SD-1}, respectively). We will follow the ideas proposed in Eq. (4) to evaluate the depolarizing field for the case of asymmetrical boundary conditions. We suppose that FLC 497 corresponds to an ideal dielectric because its conductivity is very small (its magnitude is of about 10^{-11} Ω^{-1}-cm^{-1}).

The equations for continuity of electrical displacement D and distribution of voltage supplied perpendicularly to solid substrates of a FLC cell for the case when the spontaneous polarization vector is perpendicular to substrates can be written as

$$\begin{aligned} \varepsilon_0\varepsilon_{SD-1}E_{SD-1} &= \varepsilon_0\varepsilon_{FLC}E_{FLC} + P_s \equiv D, \\ L_{SD-1}E_{SD-1} &+ d_{FLC}E_{FLC} = V. \end{aligned} \tag{13}$$

Here, E_{FLC} and E_{SD-1} are the electrical fields in the FLC and SD-1 layers, respectively, V is the voltage applied to the FLC cell, and d_{FLC} is the FLC layer thickness. From Eq. (13), one can easily find the electrical field in both layers:

$$E_{FLC} = \frac{\varepsilon_{SD-1}V - (P_s/\varepsilon_0)L_{SD-1}}{(\varepsilon_{FLC}L_{SD-1} + \varepsilon_{SD-1}d_{FLC})}$$

and (14)

$$E_{SD-1} = \frac{\varepsilon_{FLC}V + (P_s/\varepsilon_0)d_{FLC}}{(\varepsilon_{FLC}L_{SD-1} + \varepsilon_{SD-1}d_{FLC})}.$$

So, the electrical fields exist in both the FLC and SD-1 layers due to the spontaneous polarization even at V = 0, and both fields are opposite to each other in this case. Denoting

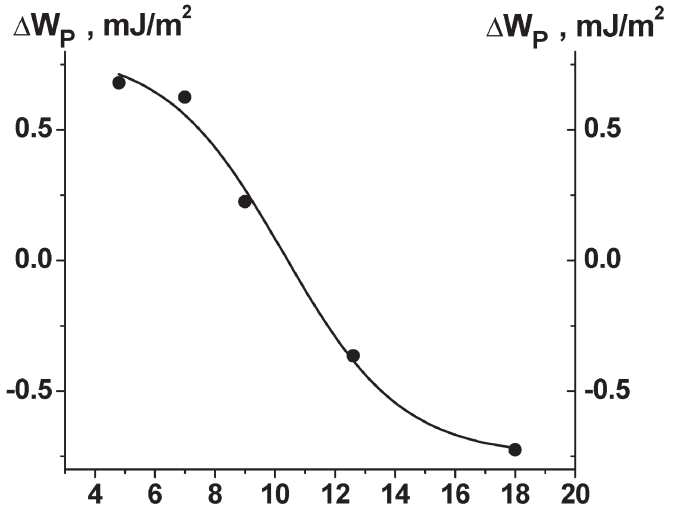


FIGURE 14 — Difference ΔW_P between the polar segments parts of the anchoring energy of FLC-497 with pure ITO and ITO covered with a SD-1 layer dependent on SD-1 layer thickness. All measurements have been carried out with an asymmetric FLC cell of 6-μm thickness for a triangular-voltage frequency f = 0.01 Hz, voltage amplitude of ±2.5 V, and temperature T = 23°C.

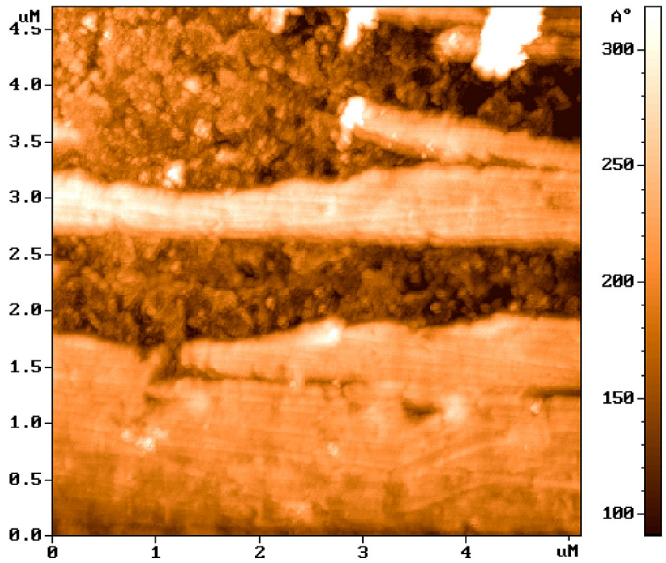


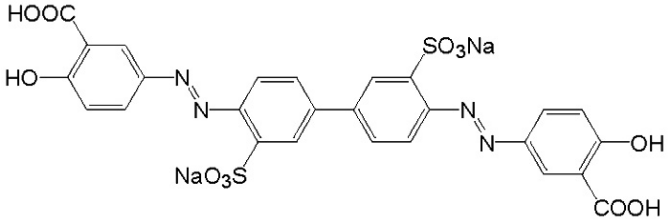
FIGURE 15 — AFM scan of ITO covered with SD-1 which was spin-coated on a ITO surface at 3000 rev/min from the SD-1 solution in DMF at a concentration 0.4%. The well-known SOLVER NT AFM technique was used for evaluation of the surface. The averaged SD-1 layer thickness was evaluated by comparative roughness analyses of a pure ITO surface and a ITO surface covered with a SD-1 layer.

these fields as $E_{FLC}{}^D$ and $E_{SD-1}{}^D$, respectively, and taking into account $d_{FLC} >> L_{SD-1}$, we have from Eq. (14):

$$E^D_{FLC} = -\frac{P_s}{\varepsilon_0 \varepsilon_{SD-1}} \cdot \frac{L_{SD-1}}{d_{FLC}}, \quad E^D_{SD-1} \frac{P_s}{\varepsilon_0 \varepsilon_{SD-1}}. \qquad (15)$$

Evidently, $E_{FLC}{}^D$ can be considered as a contribution to the apparent bias voltage applied to the FLC layer. It contributes also to the hysteresis-loop center shift, if the aligning layer is unbroken, of course. Substituting ε_{SD-1} = 7.5, d_{FLC} = 6 μm, and L_{SD-1} = 5–18 nm (see Figs. 13 and 14) into Eq. (15), we have an estimation of $E_{FLC}{}^D \cong (1.3–4.7) \cdot 10^4$ V/m at variations of unbroken aligning layers from 5 to 18 nm. A corresponding depolarizing voltage $V_{FLC}{}^D = E_{FLC}{}^D \cdot d_{FLC}$ on 6-μm FLC layer changes from 0.08 V at L_{SD-1} = 5 nm to 0.28 V at L_{SD-1} = 18 nm. By comparing these values with measured V_{sh} values, one can conclude that the depolarizing field $E_{FLC}{}^D$ does not play a decisive role in the hysteresis-loop center shift for the situation under consideration.

Actually, in our experiments the aligning layers have a just broken or a so-called island structure with typical dimensions of the islands of about several hundred nanometers, and their averaged thickness is about 10 nm, as is shown in Fig. 15. That means that the aligning layers are surface nanostructures. Changing a square of the aligning layers islands on an ITO surface results in the changing of the compensation of ITO polarity by polar groups of SD-1 layer whose chemical structure is shown below:



In fact, the aligning layers are not only island surface nanostuctures but they are conductive surfaces with the conductivity of the electronic type. It prohibits the depolarizing of a field at least inside areas of pure ITO.

So, most probably, namely the difference in polarity of the ITO and SD-1 surfaces, plays a key role in the hysteresis-loop center shift. In any case, the parameter ΔW_P defined according to Eq. (12), contains all the possible contributions including the possible depolarizing field inside the aligning islands also.

Let us note, finally, that a method of aligning surface investigations is a measurement of the contact wetting angles Θ for evaluations of the surface-free energy γ_s. It was performed by using a standard Digdrop Contact Angle Meter, GBX, supplied with corresponding software for evaluation of γ_s and correspondent polar and dispersion parts according to the Wendt–Owens equation[10]:

$$1 + \cos\Theta = \frac{2\sqrt{(\gamma_S^D \gamma_L^D)}}{\gamma_L} + \frac{2\sqrt{(\gamma_S^P \gamma_L^P)}}{\gamma_L}, \qquad (16)$$

$$\gamma_S = \gamma_S^P + \gamma_S^D, \qquad (17)$$

$$\gamma_L = \gamma_L^P + \gamma_L^D. \qquad (18)$$

Here, γ_L and γ_S are the surface-free energy (SFE) of a wetting liquid and tested solid surface, respectively; $\gamma_L{}^P$, $\gamma_S{}^P$, $\gamma_L{}^D$, and $\gamma_S{}^D$ are the polar and dispersion parts of the SFE of the liquid and surface; Θ is the static equilibrium contact angle between the solid surface and the liquid. We used

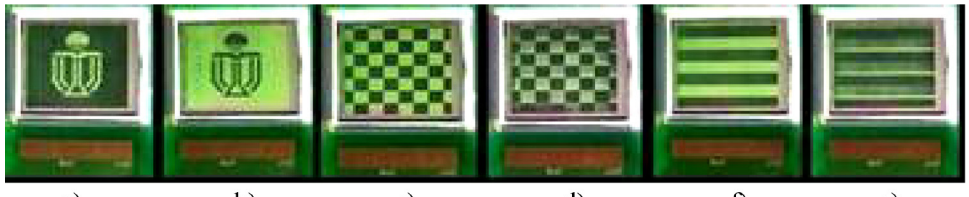


FIGURE 16 — Photographs of images memorized by a 64 × 64 FLC display matrix: (a)–(c), (f) – binary images, (d) and (f) – images with gray-scale levels.

alpha-bromonaphtalene and glycerol as wetting liquids to test the aligning surfaces.

8 Potential applications

The major potential applications is memorization of the images with gray-scale levels for an unlimited time after the driving voltage is switched off. A display prototype based on a 64 × 64- and 33 × 33-mm^2 FLC display matrix was made according to the principles discussed above to illustrate our realization (Fig. 16). Actually, any gray-scale level can be memorized. The display matrix size is 33 × 33 mm^2, and the FLC layer thickness is 5.2 ± 0.2 μm. The display device operates at a frame frequency of 30 Hz (at V_{row} = ±18 V, V_{col} = ±9 V, T = 23°C) generating a continuous gray scale, which can be memorized for more than 10 days after the driving voltage is switched off.

9 Conclusion

The origin of FLC gray scale was discussed. A new criterion for FLC bistable switching was proposed based on the FLC hysteretic behavior dependence on boundary conditions and temperature. The criteria of steady and hysteretic-free gray-scale addressing were derived. A prototype of a passively addressed FLC-based matrix display of 64 × 64 pixels has been developed, and gray-level memorization was demonstrated.

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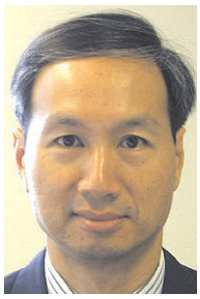

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