P-17: Metal Induced Continuous Zonal Domain Polycrystalline Silicon and Thin Film Transistors

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Abstract

Metal induced polycrystalline silicon (poly-Si) films composing of continuous zonal domain (CZD) in exactly same width have been obtained through pre-defined crystalline nucleation lines (CNL) on a nano-layer of silicon dioxide. Employing this technology, the impact of glass substrate shrinking on subsequent alignment process is determined. Additionally, the crystallization process is strictly controllable and the annealing time is shorter than one hour. P-channel thin film transistors (TFTs) built on CZD poly-Si exhibit high performance and high uniformity.

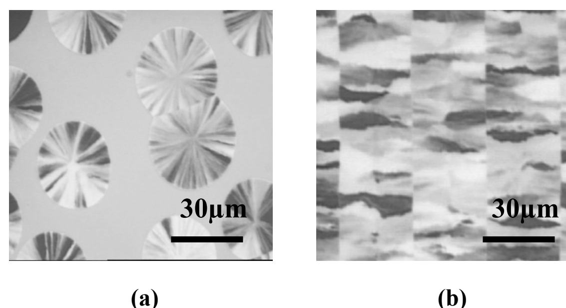
1. Introduction

Low temperature crystallization of amorphous silicon (a-Si) thin film has attracted considerable attention because of its potential applications to large area electronics on inexpensive glass substrates. Thin-film transistors (TFTs) built on metal-induced unilateral crystallized (MIUC) polycrystalline silicon (poly-Si) have been shown to exhibit high carrier mobility and good device uniformity. They can be used to realize active-matrices [1, 2] for flat-panel display and image sensor applications [3, 4].

However, MIUC-TFT [5] has problems of subsequent mask misalignment induced by glass substrate shrinking during the annealing process. Additionally, residual nickel in the poly-Si channel can affect the long term stability of the TFT. The electrical performance of MIUC TFT may shift and suffer higher off-state leakage current and early drain breakdown.

There have been several attempts to reduce the Ni content in MIC based TFT. Giant grain silicon (GGS) has been obtained by Ni-mediated crystallization of a-Si with a silicon-nitride (SiNx) cap layer [6] or using solution based metal-induced crystallization (SMIC) [7]. The problem of subsequent mask misalignment induced by glass substrate shrinking can be solved with this technology, but the random distribution of crystalline nuclei leads to longer annealing time, which is not acceptable for large area glass substrate.

A new implementation scheme which can reduce residual nickel in poly-Si as well as annealing time to less than one hour at 590℃ is proposed and demonstrated. The metal induced polycrystalline silicon (poly-Si) films composing of continuous zonal domain (CZD) in exactly same width can be obtained through pre-defining crystalline nucleation lines on a nano-layer of silicon dioxide. After the crystallization process, the entire poly-Si film can be the active layer of high performance thin film transistors (TFTs), so the impact of glass substrate shrinking on subsequent alignment process is avoided. All crystallized zonal domains have exactly the same width and length so that the crystallization process is strictly controllable and the annealing time is shorter than one hour at 590℃. Figure 1 shows the optical microscopy images of amorphous silicon films after one hour annealing at 590℃ in nitrogen (N_2) atmosphere using GGS and CZD technology respectively. The films are etched by tetra-methyl ammonium hydroxide (TMAH). As shown in Figure 1 the CZD film has been fully crystallized and the GGS film still has a lot of areas not crystallized. Figure 2 shows the average crystallization fraction over large area substrate of the film employing GGS and CZD technology as a function of the annealing time at 590℃. 100% crystallization fraction can be obtained using CZD technology at 60 mins, while that is just about 50% of the GGS technology.



(a) (b)

Figure 1. Optical microscopy images of amorphous silicon film after one hour annealing at 590°C in N_2 atmosphere employing (a) GGS technology and (b) CZD technology.

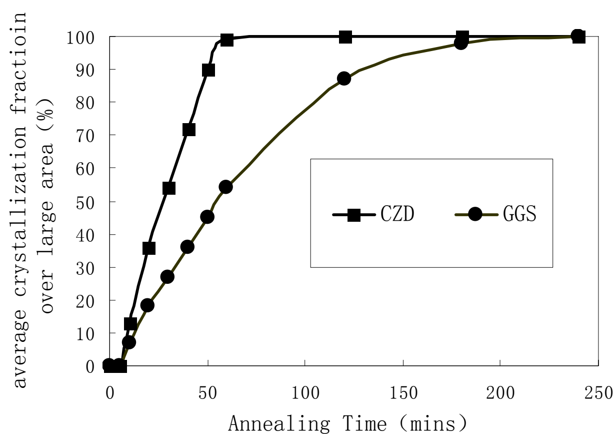


Figure 2. The average crystallization fraction over large area using CZD and GGS technology versus the annealing time at 590°C.

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This CZD process can reduce residual nickel in poly-Si films. The nickel content and distribution in crystallized CZD poly-Si film is analyzed by time of flight Secondary Ion Mass Spectrometry (Tof-SIMS). The P-channel TFTs built on this CZD poly-Si exhibit high performance and high uniformity.

2. CZD material and TFT fabrication

2.1 CZD material formation

The fabrication process began with 4-inch c-Si wafers covered with 500nm thermal oxide. Then 50nm a-Si was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. After dipping in 1% hydrogen fluoride solution (HF) for 1 minute to remove the native oxide, a SiO_2 nano-cover layer was formed on the surface of a-Si, and then it defined as lines in width of 1.5µm and apart from each other 30µm. The length of the line is equal to the width of the substrate. After the photolithography, the photo-resistor was removed by a mixed solution of H_2SO_4 and H_2O_2 at 120°C. At the same time a ~2nm layer chemical oxide was formed. Then an ultra-thin layer of nickel was sputtered on the cover layer with crystalline nuclei orientation lines. The schematic of the CZD structure was shown in Figure 3. After annealing at 590°C for 1 hour, the width of the zonal domains was half of the distance between two neighboring crystalline nucleation lines, and the length of the zonal domains is the same as the width of the substrate, which can be tens of centimeters to several meters.

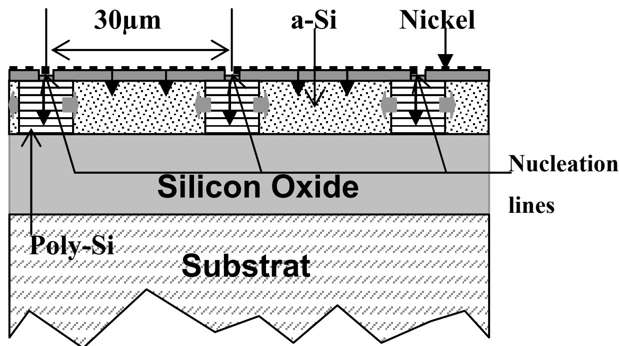


Figure 3: Cross section of the CZD structure

2.2 TFT fabrication

These CZD poly-Si films were patterned into active islands by wet etching with Freckle etchant. The freckle etchant is mainly composed of CH_3COOH, HBF_4, HNO_3 and H_3PO_4. 50nm low temperature oxide (LTO) was subsequently deposited by LPCVD at 425℃ as the gate insulator after the native oxide was removed by 1% HF. Following the deposition of 300nm aluminum which was patterned into gate electrodes, boron at a dose of $4\times10^{15}/cm^2$ was implanted into the source and drain. A 500nm LTO isolation layer was deposited and the dopants were activated at the same time. Contact holes were opened before 500nm aluminum-1%Si was sputtered and patterned as contacts. Contact sintering was then performed in forming gas at 420℃ for 30mins. The schematic cross-section of a P-channel CZD poly-Si TFT was shown in Figure 4.

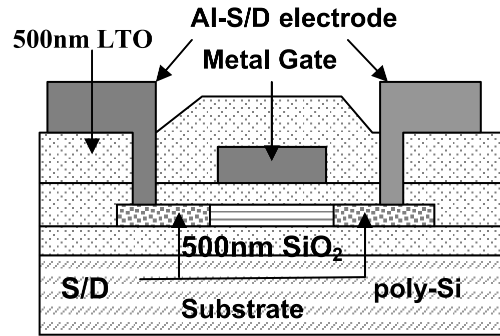
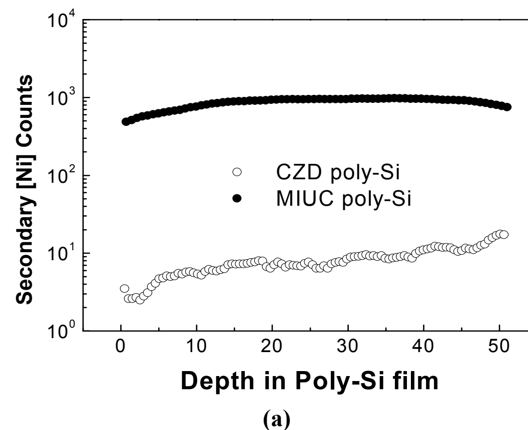


Figure 4. Schematic cross-section of a P-channel CZD poly-Si TFT

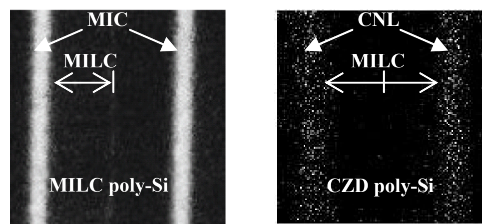
3. Results and discussion

3.1 CZD poly-Si

To compare the residual nickel concentration in CZD and metal induced lateral crystallization (MILC) poly-Si films after the crystallization process, the Ni content and distribution in CZD and MILC poly-Si films were measured by time of flight Secondary Ion Mass Spectrometry (Tof-SIMS). The nickel content in CZD film is two orders of magnitude lower than that in MILC film (Fig. 5(a)). Figure 5 (b) and (c) show the two-dimensional (2D) distribution of Ni in CZD and MILC poly-Si films respectively. Nickel and/or nickel silicide are denoted as bright dots in the 2-D images. In 2-D image of MILC poly-Si film (Fig.5 (b)), the bright columns on both sides are MIC regions and the dim line in the middle is the intersection of two MILC regions. It reveals that the nickel content is a little higher at the intersection and much higher in the MIC regions.



(a)



(b) (c)

Figrue 5. The SIMS depth profiles of nickel content (a) and 2-D image of Ni distribution in (b) MILC poly-Si film and (c) CZD poly-Si film traced by SIMS.

In the 2-D image of CZD poly-Si film (Fig.5 (c)), similar to the MIC region of MILC films, a higher Ni concentration is distributed at the crystalline nuclei lines region (CNL). But the ratio of MIC region to MILC region in MILC films was much higher than that of CNL region to MILC region in CZD films. For CZD technology, the Ni in CNL region is used for nucleation. It does not depend on the Ni diffused from the CNL. As a result, there is no area on the crystallized poly-Si which contains a very high concentration of Ni. The entire poly-Si film can be available for the active layer in TFT. So it means that the CZD poly-Si films have lower Ni concentration and higher uniformity.

3.2 TFT results and discussion

Electrical characteristics and uniformity of P-channel TFTs built on 50nm CZD poly-Si were measured with HP4156 semiconductor parameter analyzer. Firstly, transfer characteristic curves for TFTs of which W/L was 30μm/10μm with a 50nm gate insulator layer were tested. W and L denote the width and length of the transistor respectively. The field effective mobility (μ_{FE}) and the threshold voltage (V_{th}) defined as the V_g required to induce an I_d of W/L×10^{-7} at V_{ds}=-5V.

The field-effect mobility (μ_{FE}) at low drain voltage is given by

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{ds}} \qquad (1)$$

Where W and L are the effective channel width and length, g_m is the transconductance, C_{ox} is the gate insulator capacitance per unit area, V_{ds} is the voltage between drain and source. The reported field-effect mobility is the maximum value measured.

Figure 6 shows the transfer characteristics of CZD poly-Si TFTs and their field effect mobility. The p-channel CZD poly-Si TFTs exhibited a maximum field effect mobility (μ_{FE}) of 65.21cm^2/V·s, a subthreshold swing (S) of 0.56V/dec and a threshold voltage (V_{th}) of -3.5V. The a ratio of on-state to off-state drain currents is 2.6×10^7.

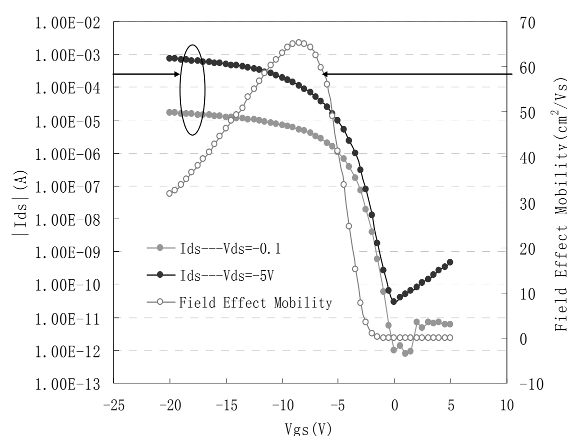


Figure 6:The drain current and field-effect mobility *vs.* gate voltage of P-type CZD-TFTs.

The uniformity of the CZD poly-Si TFTs was also studied. 20 TFTs with the same device structure distributed over the 4 inch wafer were sampled. The V_{th} and μ_{FE} of the TFTs were extracted to be analyzed and compared. Shown in Figure 7 are the distribution of the V_{th} (a) and the μ_{FE} (b) of the CZD-TFTs and GGS-TFTs. The relative scattering degree (standard deviation / average value) of field-effect mobility (ημ_{FE}) of hole is about 3.5% and 6.05% for CZDF-TFTs and GGS-TFTs respectively. A ηV_{th} of ~ 2.68% and ~ 3.72% for CZD-TFTs and for GGS-TFTs have been obtained. Obviously, a tighter distribution of field effect mobility and threshold voltage offers more controllable device performance and more stable pixel circuit. It can be seen that the uniformity of TFT devices fabricated by CZD poly-Si is superior to that of GGS-TFTs.

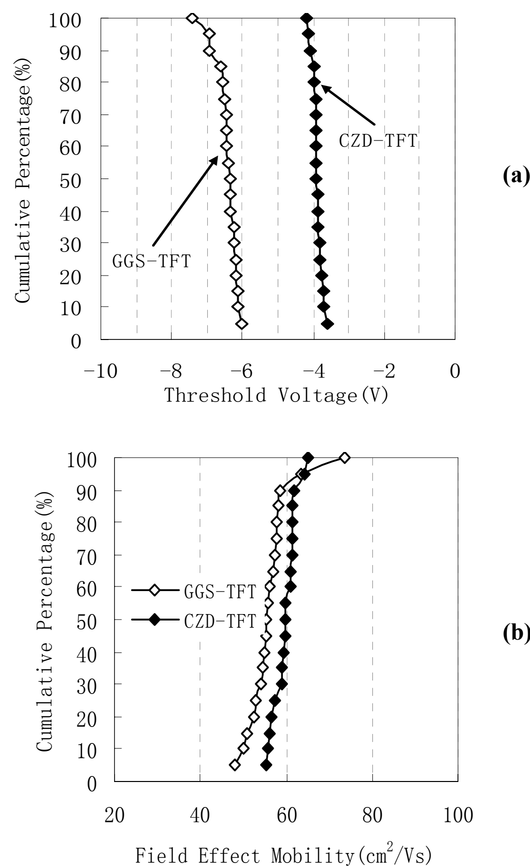


Figure 7. Statistical distribution of (a) threshold voltage, (b) field-effect mobility of p-channel CZD and GGS poly-Si TFTs.

4. Conclusion

A new implementation scheme is presently proposed to realize continuous zonal domain (CZD) polycrystalline silicon (poly-Si) films. This new technology can eliminate the impact of glass substrate shrinking on subsequent alignment process. At the same time the crystallization process is strictly controllable and make the annealing time shorter than one hour at 590℃. The P-channel TFTs built on this CZD poly-Si exhibit high performance and high uniformity.

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6. References

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