P-15: A 3 inch Active Matrix for Color Sequential- Liquid Crystal Display (CS-LCD) Based on Metal Induced Continuous Zonal Domain (CZD) Polycrystalline Silicon Technology

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ABSTRCT

Color-sequential liquid crystal display (CS-LCD) can be realized without color filter but using a field sequential LED backlight, which enables a high efficiency of backlight and low power consumption. In this paper, the fast addressing active matrix for CS-LCD is designed and fabricated with the technology of metal induced continuous zonal domain (CZD) polycrystalline silicon thin film transistors (TFTs). This panel provides fast addressing characteristics and large aperture ratio. Assembled with fast liquid crystal technology, high color purity and clear moving image can be obtained.

1. Introduction

Flat-panel display is the dominating segment of the display industry with rapid development. [1] TFT-LCD technology has a wide range of applications, from consumer products such as notebook PCs and TVs, to office products such as desktop computers monitors and PDAs. [2] Liquid-crystal display (LCD) is presently the dominant FPD technology because of its portability, low power consumption and mature manufacturing practice. High resolution, high optical efficiency, high color purity, and low cost are becoming the critical factors for LCD displays, especially for portable applications. [3]

Color representation in a conventional liquid crystal display (LCD) with color filter is realized by a combination of liquid crystal cells, micro color filters (CF) on each pixel, and a white backlight. Here, a pixel is consist of 3 sub-pixels in R, G and B, [4] as shown in Figure.1(a). 70-80% of the backlight are absorbed by the CF.[5] So in conventional LCD with CF, the efficiency of the backlight is only <10%.

A color sequential LCD reproduces R,G and B colors in a pixel in a time sequence using synchronously pulsed colored LED backlights and a liquid crystal cell without micro color filters. [6] The pixel structure is shown in Figure.1(b). This method can produce brightness display since there is no the color-filter which absorbs more than half of the backlight. The number of pixels of the color sequential display is only one third of that of a display with CF. As a result, a color sequential LCD is expected to have a higher aperture ratio (AR) than a color filter display with the same resolution, or it can realize three times higher resolution using the same technology.[7]

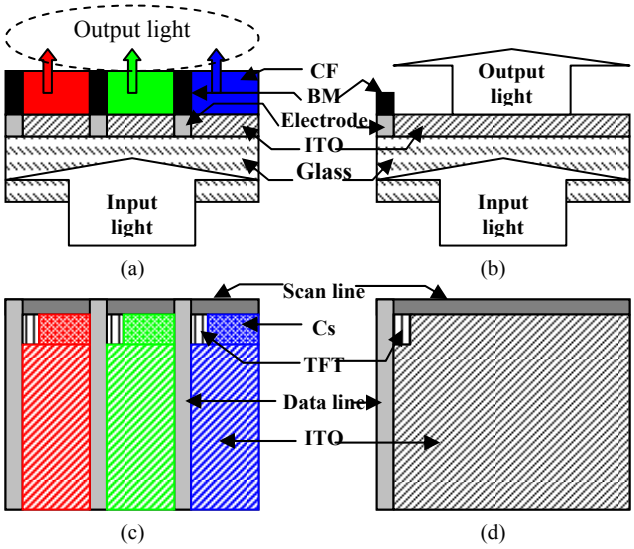

Figure 1. The schematic of cross section for traditional Color filter LCD (a) and color sequential LCD (b). Layout of the traditional Color filter LCD (c) and color sequential LCD (d) for a pixel.

The fast LCD, the programmable LCD backlight and the active matrix (AM) panel with fast addressing TFT and high aperture ratio are indispensable to fabricate CS-LCD. In this paper, we will work on the AM panel with fast addressing TFT and high aperture ratio.

2. The principle of CS-LCD

The working principle of a color-sequential LCD is by using a field sequential LED backlight. Color mixing can be achieved by controlling the on and off of the LCD when different color LED is flashing. For example, if we want to have red color, the LCD is in the off state when the red LED backlight is on and the LCD is in the on state when the green and blue LED backlight is off. By controlling the gray-level of LCD, full color display can be obtained.

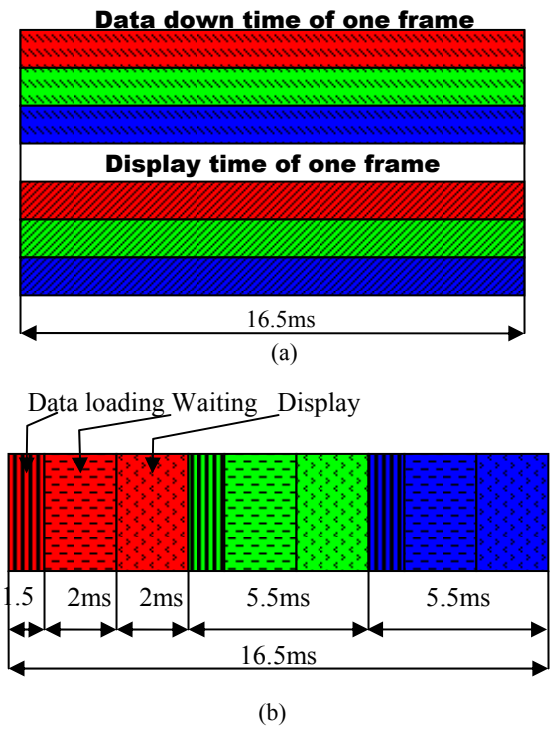

Figure 2 . Driving principle of QVGA color-filter LCD (a) and color-sequential LCD (b)

As a compensation for reduction of two thirds of pixels, each pixel of the color sequential LCD should be driven three times as fast as a conventional LCD, assuming the same frame rate. The principle of the driving for CS-LCD is shown in Figure 2(b). For a QVGA display with 60Hz frame rate, one frame can have a duration of approximate 16.5ms, which contains 3 sub-frames. The time limit for each sub-frame is only 5.5ms. The minimum response time of LCD needs 2ms and the minimum LED illumination needs about 2ms. Therefore, only around 1.5ms is left for data loading, as shown in Figure 2(b). For a color-filter LCD with the same resolution, the frame time is also around 16.5ms. The data loading, LDC response and LED illumination occurs at same time, as shown in Figure 2(a). That means the loading time for CS-LCD is ten times of that for color filter LCD assuming the same resolution.

3. Design of the pixel TFT

First we analyze what is required of the pixel TFT in AM CS-LCD. With V_D representing the voltage on the data line, the voltage level on the pixel as a function of time (t) is approximately described by the following equations:

$V_{write} = V_D(1 - e^{-t/\tau_{on}}); \quad \tau_{on} = R_{on}C_s$ ..... (1) When selected and,

$V_{hold} = V_D e^{-t/\tau_{off}}; \quad \tau_{on} = R_{off}C_s$ ..... (2) When not selected.

R_{on} and R_{off} are the resistance of the pixel TFT in the "on" and "off" states, respectively. V_{write} and V_{hold} are the voltage on the pixel electrode at charging process and holding process.
When writing images to the LC, it requires

$V_{signal} \succ 0.99V_D \Rightarrow T_{writing} \succ 4.6\tau_{on}$ ..... (3)

In the images holding process, it requires

$V_{signal} \succ 0.95V_D \Rightarrow T_{holdign} \prec \tau_{off} / 19.5$ ..... (4)

So, $\tau_{on} \prec T_{writing} / 4.6 \Rightarrow R_{on} \prec T_{writing} / 4.6C_s$ ..... (5)

$\tau_{off} \succ 19.5T_{holding} \Rightarrow R_{off} \succ 19.5T_{holding} / C_s$ ..... (6)

V_{signal} is the image voltage on the pixel electrode, $T_{writing}$ is the time of writing the image and $T_{holding}$ is the time of holding the image, this is a typical frame period in display standard. In AM CS-LCD display C_s is ~ 1.0pF in the present design. As mentioned before, the time limit for each sub-frame is only 5.5ms. So the holing time is 5.5ms, the R_{off} should be $R_{off} \succ 19.5T_{holding} / C_s = 1.07 \times 10^{11}\Omega$.

The color sequential LCD should be driven three times as fast as a conventional LCD at the same frame rate. The writing time is only about 1.5ms, so it requires much smaller R_{on} than the conventional LCD. For the address TFT, it works in the linear region, the drain current (I_d) is given by

$$I_{ds} = \mu_{FE} \frac{\varepsilon_0 \varepsilon}{t_{ox}} \times \frac{W}{L}\left(V_{gs} - V_T\right) \times V_D \quad \text{..... (7)}$$

$$\Rightarrow R_{on} = \frac{V_D}{I_{ds}} = \frac{t_{ox}L}{\mu_{FE}\varepsilon_0\varepsilon W\left(V_{gs} - V_T\right)} \quad \text{..... (8)}$$

where μ_{FE} is the field-effect mobility, $\varepsilon_0\varepsilon$ is the dielectric constant of gate oxide, W and L are the respective width and length of the TFT, V_{gs} is the applied gate to source voltage and V_T is the threshold voltage. Combine with the equation (5), the ratio of width to length (W/L) of TFT can be written as

$$\frac{W}{L} \succ \frac{4.6 \times C_s t_{ox}}{\mu_{FE}\varepsilon_0\varepsilon\left(V_{gs} - V_T\right) \times T_{writing}} \quad \text{..... (9)}$$

Here, we assume at "on" state, the V_{gs} of the TFT is 15V and $C_s = 1.0\text{pF}$. With the parameters of the a-Si:H TFT and Poly-Si TFT listed in table □, the required ratio of channel

width (W) to length (L) of the TFT can be derived with equation (9), as listed in tale□. For a QVGA display with 60Hz frame rate, the writing time is 6μs for every pixel. The ratio of W/L of a-Si:H TFT requires at least 9.3. At the same time, the ratio of W/L of Poly-Si TFT requires only 0.1. That means for the 5μm process, the width of the TFT channel is 50μm for a-Si:H TFT and only 0.5 For poly-Si TFT. For higher resolution display, the writing time decreases, so the TFT with larger W/L ratio is required. Taking SXGA display for example, the limited writing time is only 1.4μs. The channel width of a-Si:H TFT requires at least 200μm based on 5μm process that is totally impossible. Compared to a-Si:H TFT, higher aperture ratio (AR) can be reached using poly-Si TFT due to the higher field effect mobility.

Table Ⅰ： Typical parameters of Poly-Si TFT and a-Si:H TFT

	μ_{Max} (cm^2/Vs)	$\mu_{Work\ point}$ (cm^2/Vs)	Gate Insulator	T_{ox} (nm)	ε
a-Si:H TFT	0.8	0.4	SiNx	300	7.0
Poly-Si TFT	60	30	LTO	120	4.0

Here, assuming the pixel size is fixed at 200μm×200μm, the width of both scan line and data line is 12μm. The smallest space at same layer is 5μm, and the lateral smallest space for different layer is 2μm. Normally, the gate length of TFT is 5μm or 10μm in LCD display. Based on these process parameters the typical layout for a pixel, which has only one TFT, the ratio of W/L of TFT for different resolution employing a-Si:H TFT and poly-Si TFT are listed in table II. Figure 3 shows the aperture ratio (AR) as a function of the number of scan line using a-Si:H TFT and poly-Si TFT as addressing TFT based on 5μm and 10μm process respectively. For the a-Si:H TFT, the AR of pixel decreases with the increasing of scan lines. For poly-Si TFT, the AR of pixel almost maintains at 77%-78%. So the poly-Si TFT is necessary for achieving high resolution and high AR display.

Basing on the calculation on the LC holding process, assuming the capacitance of LC is about 1pF, the maximum holding time for above situation is 4ms. That means the capacitance of LC is large enough for the QVGA CS-LCD with 60Hz frame rate. So, there is no need additional storage capacitance for AM CS-LCD.

Table Ⅱ. The ratio of width to length of addressing TFT

Resolution	Rows (lines)	$T_{writing}$ (μs)	W/L (a-Si:H TFT)	W/L (P-Si TFT)
QVGA	240	6.0	9.3	0.1
VGA	480	3.0	18.6	0.2
XGA	768	1.8	3.1	0.4
SXGA	1024	1.4	39.9	0.5

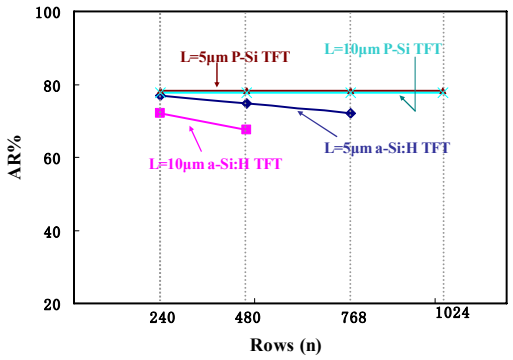

Figure 3. The aperture ratio (AR) as a function of the number of scan lines using a-Si:H TFT and P-Si TFT based on 5μm and 10μm process respectively.

4. Fabrication for Active Matrix

Basing on the above design, the panel fabrication started with the deposition of 300nm silicon oxide using plasma enhanced chemical vapor deposition (PEVCD) on Eagle 2000 glass substrate. After annealing at 590 ºC for 4 hours, the a-Si:H was fully crystallized to continuous zonal domain (CZD) polycrystalline silicon[8]. These CZD poly-Si films were patterned into active islands by wet etching with Freckle etchant. 50nm low temperature oxide (LTO) was subsequently deposited by LPCVD at 425 ºC as the gate insulator after the native oxide was removed by 1% HF. Following defining gate electrodes and the scan line, boron at a dose of $4\times10^{15}/cm^2$ was implanted into the source and drain. A 500nm PECVD oxide as isolation layer was deposited and contact holes were opened on the gate electrode. Subsequently, 700nm aluminum-1%Si was sputtered and patterned to form the inter-connections. Contact sintering was then performed in forming gas at 420 ºC for 30mins and the dopants were activated at the same time. The pixel electrode indium thin oxide (ITO) was patterned by lift-off process. Finally the black matrix was defined to reduce the reflection of Al electrode. The panel was the ready for LCD integration.

Electrical characteristics of CZD poly-Si TFTs were measured with HP4156 semiconductor parameter analyzer. Transfer characteristic curves and their field effect mobility (μ_{FE}) of TFTs are shown in Figure 4. The threshold voltage (V_{th}) is defined as the V_g required to induce an I_d of W/L×10^{-7} Å at V_{ds}=-5V. The field-effect mobility (μ_{FE}) at low drain voltage is given by

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{ds}}$$

Where W and L are the effective channel width and length, g_m is the transconductance, C_{ox} is the gate insulator capacitance per unit area, V_{ds} is the voltage between drain and source. The reported field-effect mobility is the maximum value measured.

The p-channel CZD poly-Si TFTs exhibited a maximum field effect mobility (μ_{FE}) of 65.21cm^2/V·s, a subthreshold swing (S) of 0.56V/dec and a threshold voltage (V_{th}) of -3.6V. The on state current and off state current of the TFTs are 7.36×10^{-4}Å and 4.1×10^{-11} Å respectively. The ratio of on-state to off-state drain current is 2.6×10^7.

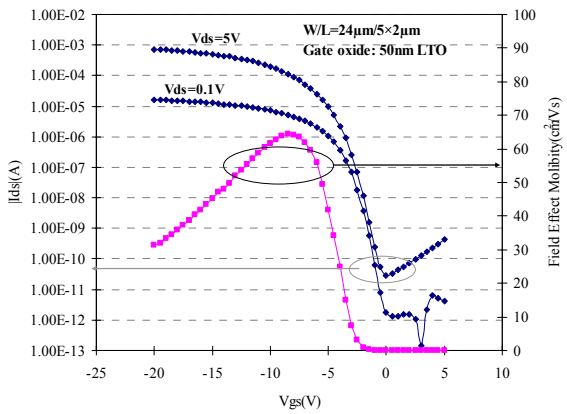

Figure 4.Ttransfer characteristic curve and the field effect mobility (μ_{FE}) for TFTs.

Figure 5 shows the representative image from the 3-inch QVGA active matrix CS-LCD.

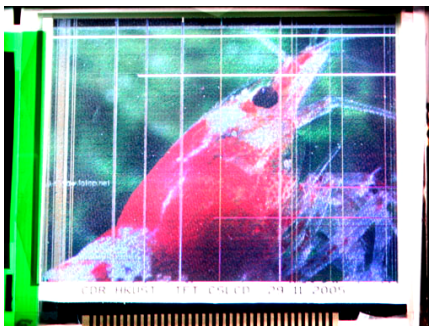

Figure 5. The representative image from the 3-inch QVGA active matrix CS-LCD

4. CONCLUSION

3 inch QVGA Active Matrix for CS-LCD was designed. It was fabricated using the technology of metal induced continuous zonal domain (CZD) polycrystalline silicon thin film transistors (TFTs). The display realizes good colors and fluent video display.

5. ACKNOWLEDGEMENT

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