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Investigation of Disk-Like Domain Polycrystalline Silicon Films and Thin-Film Transistors Using Solution-Based Metal Induced Crystallization

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Abstract: Polycrystalline silicon (poly-Si) films consisting of super-large disk-like domains were obtained with solution-based metal-induced crystallization (SMIC) of amorphous silicon. The prepared disk-like domain SMIC poly-Si has an average domain size of up to 50 μm, highest hole Hall mobility of 30.8 $cm^2/V\cdot s$, and highest electron Hall mobility of 45.6 $cm^2/V\cdot s$. P-type poly-Si TFT based on disk-like domain SMIC poly-Si has high field effect mobility of 70~80 $cm^2/V^{-1}\cdot s^{-1}$, sub-threshold slope of 1.5 V/decade, on/off state current ratio of 1.01×10^7 and threshold voltage of -8.3 V. Also, P-type disk-like domain SMIC poly-Si TFTs exhibited excellent reliability under high gate bias-stress and hot carrier bias-stress.

Key words: disk-like domain SMIC poly-Si; poly-Si TFTs; TFT reliability

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1 Introduction

While most active matrix liquid crystal displays (LCD) are made of amorphous silicon (a-Si) thin film transistors (TFT), there is always a demand for polycrystalline silicon (poly-Si) based active matrix displays because the latter can provide much higher resolution and smaller pixels. As well, some of the driver circuitry can be integrated onto the glass substrate in the case of poly-Si TFT. Additionally, poly-Si TFT is more stable than a-Si TFT in terms of driving organic light emitting diode (OLED) displays. Thus low cost, high performance and reliable low temperature poly-Si (LTPS) processing technologies are greatly required[1,2].

Poly-Si films with large crystalline grains have been obtained using the techniques of excimer laser annealing (ELA)[3] and metal-induced crystallization (MIC)[4]. There are several variations of MIC such as metal induced lateral crystallization (MILC) and metal induced unilateral crystallization (MIUC). We refer to all of them as MIC in the following. ELA is capable of producing poly-Si films with low defect density and high mobility. However, it suffers from inhomogeneity of film, high initial equipment cost, high maintenance cost, and high process complexity. MIUC poly-Si TFTs employing annealing at 550 ℃ has been studied[5]. Although capable of high performance and good uniformity, MIUC TFT needs an additional mask to define the crystallization-inducing windows, which makes the process more complicated and higher

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cost. Additionally, residual nickel in the poly-Si channel affects the long-term stability of the TFT. So poly-Si TFTs with reduced fabrication complexity, high performance, reliability and uniformity is the key factor of its practicality [6].

There have been several attempts to reduce the Ni content in MIC based TFT. Disk-like poly-Si silicon has been obtained by Ni-mediated crystallization of a-Si with a silicon-nitride (SiN_x) capping layer [7]. In this process, Ni was sputtered onto the SiN_x/a-Si layer and then annealed at around 600 ℃. The capping SiN_x layer controlled the Ni content inside the MIC layer to acceptable limit, however, that process is quite complicated. It costs more because of the vacuum process involved and the requirement to remove the capping layer afterwards.

In this paper, we discuss a solution-based MIC (SMIC) process for the fabrication of poly-Si TFT. The disk-like poly-Si film with low Ni content is obtained by controlling the Ni adsorption process in the $Ni(NO_3)_2$/NH_4OH mixed solution. Therefore, poly-Si TFT with good performance and high reliability can be obtained.

2 Results and Discussion

2.1 SMIC Poly-Si Film

The fabrication process began with 101.6 mm (4 in) c-Si wafers covered with 500 nm thermally-oxided layer. Then 50 nm a-Si was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 ℃. After dipping into 1 % hydrogen fluoride (HF) solution for 1 min to remove the native oxide, the sample was immersed in a $w = 1 \times 10^{-5}$ (quality ratio of nickel nitrate crystalline to deionized water) nickel nitrate ($Ni(NO_3)_2$) solution with a pH value of 8. The pH value was adjusted by adding a small amount of ammonia (NH_4OH). The samples were then annealed at 590 ℃ for 6 h in nitrogen ambience and were fully crystallized. When the immersion time was 2 min, a disk-like domain structure with a typical diameter of 30～50 μm was obtained, as shown in Fig. 1 (a). When the immersion time was increased to 10 min, the domain structure became floc-like, as shown in Fig. 1(b). Between 2～10 min, for example, for 5 min, two types of domains were found in the poly-Si film.

It was observed that the reproducibility and the uniformity of the crystallized poly-Si were sensitive to the pH value of the mixed solution. The pH value of the $Ni(NO_3)_2$ solution, which is approximately 6 under normal conditions, can be increased to 10 by adding NH_4OH. The crystallization of a-Si was more reproducible in terms of average domain size if immersed in $Ni(NO_3)_2$/NH_4OH mixed solution with pH value from 7 to 9, but random and non-uniform if immersed in unmodified $Ni(NO_3)_2$. The surface of a-Si was damaged if the pH value was higher than 9 [8]. So the pH value of the $Ni(NO_3)_2$/NH_4OH mixed solution was always kept at 8 in our experiments.

Because of the etching selectivity of tetramethyl ammonium hydroxide (TMAH) etchant between different crystalline orientations, the etched poly-Si by TMAH at room temperature showed the inside structure of the films. The morphologies of SMIC poly-Si were studied using this technique. Two distinctly different kinds of structures were observed and shown in Fig. 1.

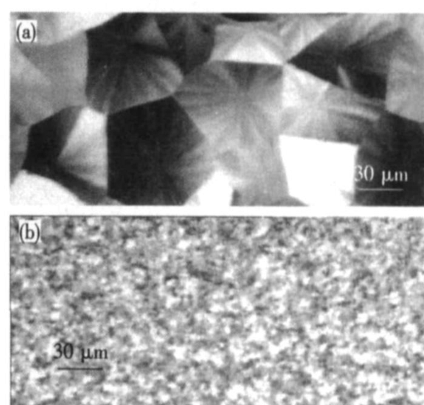

Fig. 1 Optical microscopy images of the full crystallized SMIC poly-Si etched by TMAH. (a) Disk-like domain and (b) Floc-like domain.

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They correspond to immersion times of 2 min and 10 min, respectively. Fig. 1 (a) shows the disk-like domains and the obvious colliding grain boundaries. The average domain size was about 30～50 μm. The floc-like domains and ambiguous grain boundaries were shown in Fig. 1 (b), where the average domain size was about 3～5 μm.

2.2 Hall Mobility Measurement

In order to measure Hall mobility, the fully crystallized SMIC poly-Si films were implanted with phosphorus and boron at different dosage of 8×10^{13}, 2.0×10^{14}, 5×10^{14} atoms/cm^2 for various samples. Then the samples were post-annealed at 590 ℃ for 3 h for activation.

As shown in Fig. 2, the highest Hall mobility of P-type poly-Si which was obtained at an implantation dosage of 1×10^{14} atoms/cm^2 (corresponding to 2×10^{19} atoms/cm^3) was 30.8 cm^2/V·s of disk-like domains and 22.5 cm^2/V·s for floc-like domains, respectively. With the implantation dose increasing up to 2.5×10^{14} atoms/cm^2 (corresponding to 5×10^{19} atoms/cm^3), the hole Hall mobility decreased to 27.1 cm^2/V·s for disk-like domains and 22.3 cm^2/V·s for floc-like domains. From these results, it can be seen that the Hall mobility of disk-like P-type poly-Si was much higher than that of floc-like

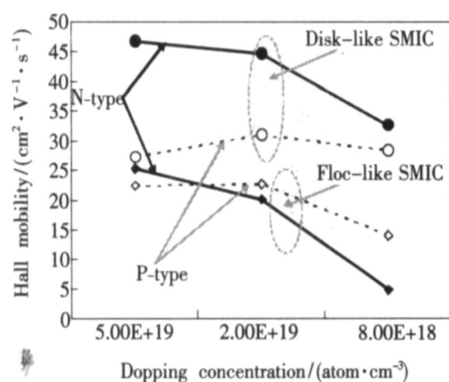

Fig. 2 Hall mobility of the disk-like domain and floc-like domain SMIC poly-Si, which were implanted separately with phosphorus and boron at different regions at dose of 8×10^{13}, 2.0×10^{14}, 5×10^{14} atoms/cm^2 respectively.

domain poly-Si, and it decreased a little as the impurity concentration was increased. It can be confirmed that the disk-like domain poly-Si has better crystallization quality, lower defect density and less grain boundaries compared to floc-like domain poly-Si [9].

For N-type SMIC poly-Si, its Hall mobility increased with the increasing of the impurity concentration until the impurity concentration reached 5×10^{19} atoms/cm^3. The Hall mobility of disk-like domain and floc-like domain poly-Si was 46.5 cm^2/V·s and 25.2 cm^2/V·s respectively when the impurity concentration was 5×10^{19} atoms/cm^3. The Hall mobility of phosphorus-doped SMIC poly-Si does not have the same trend as that for the boron-doped material. There might be two possibilities. First, phosphorus and boron were doped at the same dosage, due to the difference of atom mass, the SMIC poly-Si films finally got different carrier concentration after the same activation process. Second, the defects and grain boundaries or the residual nickel in the SMIC poly-Si have more effect on the motion of electrons than that of holes [10].

2.3 SMIC Poly-Si TFT

The SMIC poly-Si films with two different kinds of structure, disk-like domain and floc-like domain, were patterned into active islands, and unwanted poly-Si was etched away using Freckle etchant. 100 nm low temperature oxide (LTO) was subsequently deposited using LPCVD at 425 ℃ as gate insulator after the native oxide was removed by 1 % HF. Later 280 nm LPCVD poly-Si was deposited and patterned into gate electrodes. Boron with the dose of 4×10^{15}/cm^2 were implanted into the source, drain and gate regions of P-type TFTs. 500 nm LTO isolation layer was deposited and the dopants were activated at the same time. Contact holes were opened before 700 nm m(Al) : m(Si) = 1 : 100 film was sputtered and patterned. Contact sintering was performed in forming gas at 420 ℃ for 30 min. Fig. 3 shows the schematic cross-section of a P-channel

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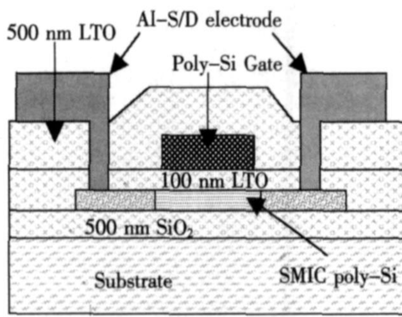

Fig. 3 Schematic cross-section of a P-channel SMIC poly-Si TFT

SMIC poly-Si TFT.

Electrical characteristics of P-channel TFTs fabricated with SMIC poly-Si films as active layer were measured with HP4156 semiconductor parameter analyzer. Transfer characteristic curves were measured for TFTs with $W/L = 30\ \mu m/10\ \mu m$. W and L denote the width and length of the transistor respectively. The threshold voltage (V_{th}) are defined as the V_g required to induce an I_d of $W/L \times 10^{-8}$ A at $V_{ds} = -0.1$ V. The field-effect mobility (μ_{FE}) at low drain voltage ($V_{ds} = -0.1$ V) is given by $\mu_{FE} = \frac{L g_m}{W C_{ox} V_{ds}}$,where W and L are the effective channel width and length, g_m is the transconductance, C_{ox} is the gate insulator capacitance per unit area, V_{ds} is the voltage between drain and source. The reported field-effect mobility is the maximum value measured.

Fig. 4 shows the transfer characteristics of disk-like domain and floc-like domain SMIC poly-Si TFTs and their field-effect mobility. The P-channel TFTs with disk-like domain SMIC poly-Si exhibited a field effect mobility of 73.8 $cm^2/V\cdot s$, sub-threshold slope of 1.5 V/decade, on/off state current ratio of 1.01×10^7 and threshold voltage of -8.3 V. At the same time, the P-channel floc-like domain SMIC poly-Si TFTs showed a field effect mobility of 46.9 $cm^2/V\cdot s$, sub-threshold slope of 1.86 V/decade, on/off state current ratio of 0.82×10^7 and threshold voltage of -10.1 V. Therefore, from the performance comparison, we can see that, the performance of SMIC poly-Si TFTs is mainly determined by the domain structure of the poly-Si films.

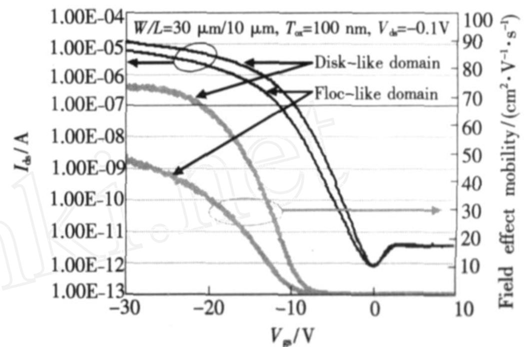

Fig. 4 Drain current and field-effect mobility *vs.* gate voltage of p-type TFTs fabricated with of disk-like domain and floc-like domain SMIC poly-Si

2.4 Bias Stability of SMIC TFT

Fig. 5 (a) and (b) show the gate bias-stress effects on field effect mobility and threshold voltage of P-channel disk-like domain SMIC poly-Si

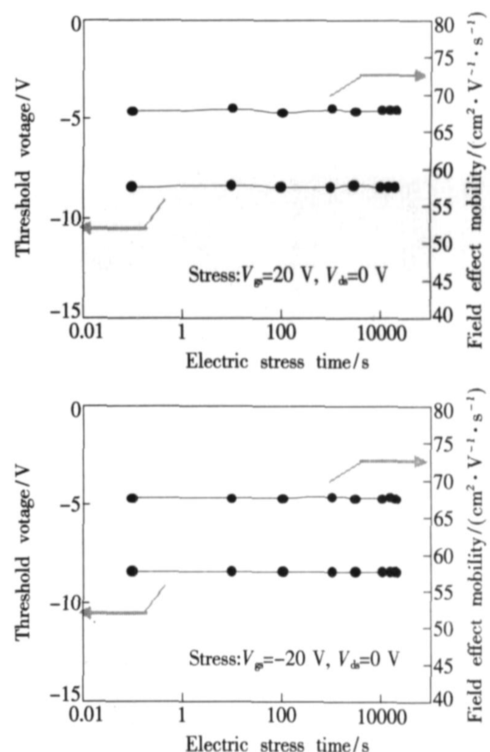

Fig. 5 Positive and negative gate-bias stress (at $V_{gs} = \pm 20$ V) effects on the field-effect mobility variation and the threshold voltage shift for P-channel disk-like domain SMIC poly-Si TFT

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TFTs under the bias of $V_{gs}=20$ V, $V_{ds}=0$ V and $V_{gs}=-20$ V, $V_{ds}=0$ V respectively. In poly-Si TFT, gate stress induces electron (hole) trappings for positive (negative) gate bias stress into the SiO_2. From Fig. 5, we can see that, for the P-channel disk-like domain SMIC poly-Si TFT, there is no change in the threshold voltage and field-effect mobility, which means that there is neither weak bond breaking such as Si—Si, Si—O nor carrier trapping into the oxide at the Si/SiO_2 interface by gate bias stress. We can say that the P-channel disk-like SMIC poly-Si TFTs exhibited excellent reliability undergoing the gate-bias stress.

Fig. 6 shows the comparison of the shifts in the field effect mobility and threshold voltage as a function of hot carrier bias-stress time at $V_{gs}=-15$ V and $V_{ds}=-30$ V for P-channel disk-like domain SMIC poly-Si TFTs. The performance of a poly-Si TFT can be degraded by hot carrier-induced

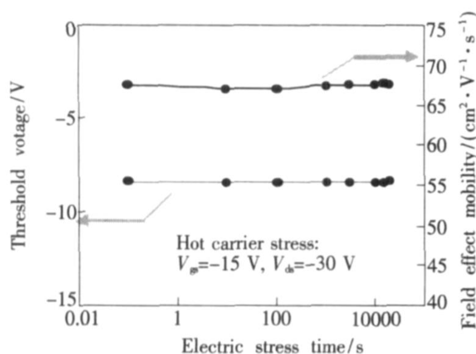

Fig. 6 Hot carrier bias-stress effect on the field-effect mobility variation and the threshold voltage shift for the P-channel disk-like domain SMIC poly-Si TFT versus bias stress time

defect creation within the channel. The bias induced change can be seen in a-Si:H and poly-Si devices, where carriers are believed to break weak silicon-silicon bonds or/and silicon-hydrogen bonds [11]. Mid gap state creation by bond breaking gives a parallel shift in the transfer characteristics without significant change in the field effect mobility [12]. According to our experimental results, there is no change in the threshold voltage, field-effect mobility, and the sub-threshold slope for the P-channel disk-like domain SMIC poly-Si TFT.

3 Conclusion

Disk-like domain poly-Si films were obtained with solution-based metal-induced crystallization (SMIC) of amorphous silicon. The SMIC poly-Si has an average domain size of up to 50 μm, highest hole Hall mobility of 30.8 $cm^2/V\cdot s$, and highest electron Hall mobility of 45.6 $cm^2/V\cdot s$. P-channel poly-Si TFT based on disk-like domain SMIC poly-Si has high field effect mobility of 70～80 $cm^2/V\cdot s$, sub-threshold slope of 1.5 V/decade, on/off state current ratio of 1.01×10^7 and threshold voltage of -8.3 V. The P-channel MIC poly-Si TFTs had very stable performance against gate bias-stress as well as hot carrier-bias stress. Therefore, with the disk-like domain poly-Si film as active layer, P-channel TFTs have good performance, and high reliability, which is the promising technology to realize the low cost, simple process poly-Si circuit and flat-panel displays.

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基于溶液法的金属诱导碟型晶畴多晶硅薄膜和薄膜晶体管的研究

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摘　要

以非晶硅为晶化前驱物,采用镍盐溶液浸沾的方法可以得到超大尺寸碟型晶畴结构的低温多晶硅薄膜。所得多晶硅薄膜的平均晶畴尺寸大约为 50 μm,空穴的最高霍尔迁移率为 30.8 $cm^2/V \cdot s$,电子的最高霍尔迁移率为 45.6 $cm^2/V \cdot s$。用这种多晶硅薄膜为有源层,所得多晶硅 TFT 的场效应迁移率典型值为 70～80 $cm^2/V \cdot s$,亚阈值斜摆幅为 1.5 V/decade,开关电流比为 1.01×10^7,开启电压为 -8.3 V。另外,P 型的 TFT 在高栅偏压和热载流子偏压下具有良好的器件稳定性。

关　键　词:碟型晶畴多晶硅薄膜; 多晶硅 TFTs; TFT 稳定性

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