P-26: Self-aligned Top-gate ZnO Thin Film Transistor with Novel Al_2O_3/SiO_2 Gate Insulator Structure

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Abstract

A novel Al_2O_3/SiO_2 gate insulator structure is developed for realizing a high performance self-aligned top-gate ZnO thin film transistor. After the sputtering of ZnO thin film, an Al_2O_3 protective layer is sputtered immediately on top of the ZnO layer in the same sputtering chamber without breaking the vacuum, which protects the surface of ZnO active layer from exposing to air or solution in the later process. With minimized charge trapping at the interface between the channel layer and the gate dielectric, the resulting transistor exhibits a field effect mobility of 27 cm^2/Vs, a threshold voltage of 1.2 V, a subthreshold swing of 0.25 V/decade and an on/off current ratio of 10^6. Good short channel characteristics are also obtained with a small shift of the threshold voltages and no degradation of subthreshold swing.

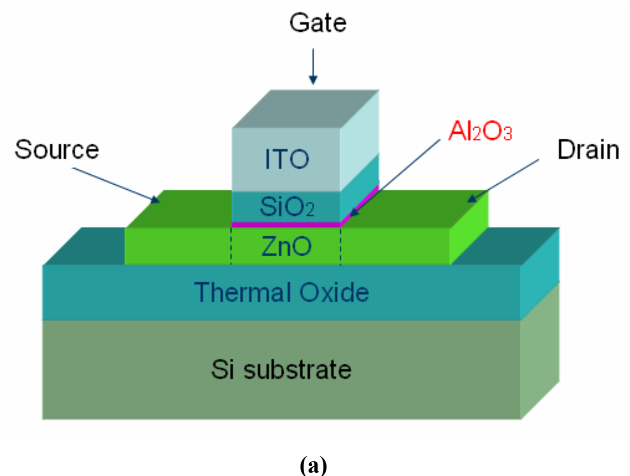
1. Introduction

Recently, Zinc Oxide (ZnO) has attracted wide attention with its notable advantages over the other semiconductors including a wide direct band gap of 3.37 eV, high transparency in the visible range (400-700 nm), good thermal stability, large exciton binding energy (60 meV) and high mobility. Therefore, ZnO thin film transistor (TFT) has become attractive for use as driving devices in large scale active-matrix organic light-emitting diode (AMOLED) applications, due to their better reliability and performance including high mobility, excellent subthreshold gate voltage swing, and high on/off current ratios, as compared to a-Si TFTs [1-4]. A bottom-gate structure is widely studied. But this structure is unsuitable for the realization of complementary metal-oxide-semiconductor gates for digital and analogy circuits because it has a high parasitic capacitance and poor scalability. Therefore, the development of a self-aligned top-gate ZnO TFT is necessary.

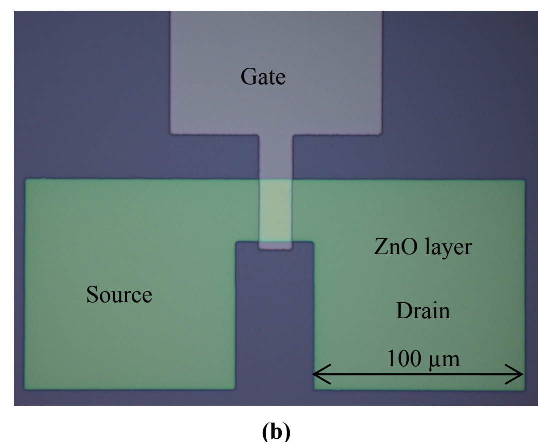
In a typical top-gate structure process [5], after the sputtering of ZnO thin film, the surface of this ZnO active layer will be exposed to air or solution in the etching or lift-off process, which leads to a poor interface between the ZnO channel layer and the gate dielectric. In this paper, a novel Al_2O_3/SiO_2 gate insulator structure is developed to minimize the charge trapping at the interfaces due to the Al_2O_3 buffer layer, which is sputtered on top of the ZnO layer immediately after the sputtering of the ZnO thin film without breaking the vacuum. The resulting ZnO TFT has a field effect mobility of 27 cm^2/Vs, a threshold voltage of 1.2 V, a subthreshold swing of 0.25 V/decade and an on/off current ratio of 10^6. With scaling down of the channel length, good characteristics are also obtained with a small shift of the threshold voltages and no degradation of subthreshold swing.

2. Experiments

The cross-sectional schematic and optical micrograph of the self-aligned top-gate type ZnO TFT studied in this paper are shown in Figure 1.



(a)



(b)

Figure 1. (a) A cross-section schematic, and (b) optical micrograph of the proposed ZnO TFT with top-gate structure.

A 100nm thick ZnO active layer was first sputtered on thermally oxidized silicon wafer by radio frequency magnetron sputtering (120 W) using a single ZnO target in a mixed Ar and O_2 ambient (Ar/O_2=9:1) at room temperature. Then, a very thin Al_2O_3 protective layer was sequentially sputtered on top of the ZnO layer using the same sputtering machine without breaking the vacuum.

After patterning of these two layers by lift-off technique, a 100nm thick SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) at 300ºC on top of the active layer. A 100nm thick indium tin oxide (ITO), used as gate electrode, was sequentially sputtered at room temperature. After patterning of the ITO electrode by lift-off technique, the Al_2O_3/SiO_2 gate stack was continuously dry etched using ITO as a mask. This process was followed by Ar plasma treatment [6] and hydrogen plasma treatment [7] sequentially on the source/drain region of the ZnO TFT, which lead to a low sheet resistance and a low contact resistance between the source/drain electrodes and the channel of the active layer. No further annealing is needed in the whole process. The electrical properties of the TFTs were measured using an Agilent 4145B parameter analyzer.

3. Results and Discussion

Figure 2 shows the X-ray diffraction (XRD) pattern of the ZnO thin film deposited at room temperature and the 2θ peak corresponding to (002) was observed at 34.2º, indicating that the ZnO film has a *c*-axis orientation. Calculated from the Scherrer formula, the estimated average grain size of the deposited ZnO thin film is around 8 nm.

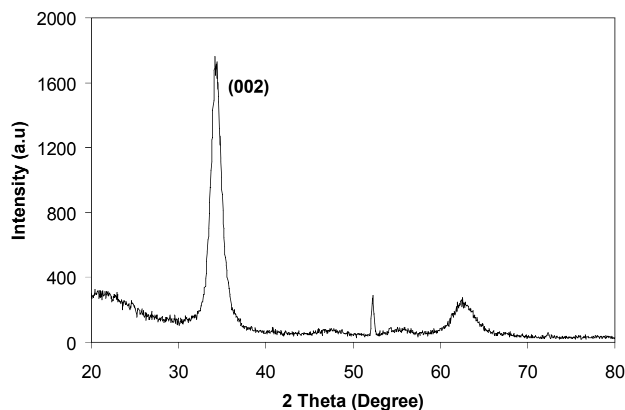


Figure 2. The XRD pattern of the ZnO thin film deposited on thermally oxidized silicon substrate.

Figure 3 shows the transfer characteristics of the fabricated ZnO TFTs with a width to length ratio of 30/16 µm. They exhibit good transfer TFT characteristics at a drain voltage of 5 V such as a field effect mobility of 27 cm^2/Vs, a threshold voltage of 1.2 V, a subthreshold swing of 0.25 V/decade and an on/off current ratio of 10^6. The linear mobility of 25 cm^2/Vs is also obtained at a drain voltage of 0.2 V. The linear mobility and saturate mobility obtained are nearly comparable, implying that the field-effect mobility is independent on V_D. All transistors studies here have low leakage current I_G<10 pA.

In general, the subthreshold swing value is an indicator of the total trap density including the bulk trap density of the ZnO layer itself and the interface trap density at or near the interface between ZnO and Al_2O_3. The good subthreshold swing for the ZnO TFTs demonstrates that the proposed Al_2O_3/SiO_2 gate insulator structure proposed here can minimize the charge trapping at the interface effectively due to the Al_2O_3 buffer layer. Compared with the reported performance of other ZnO TFTs [1-4, 8, 9], the proposed ZnO TFTs exhibits higher performance.

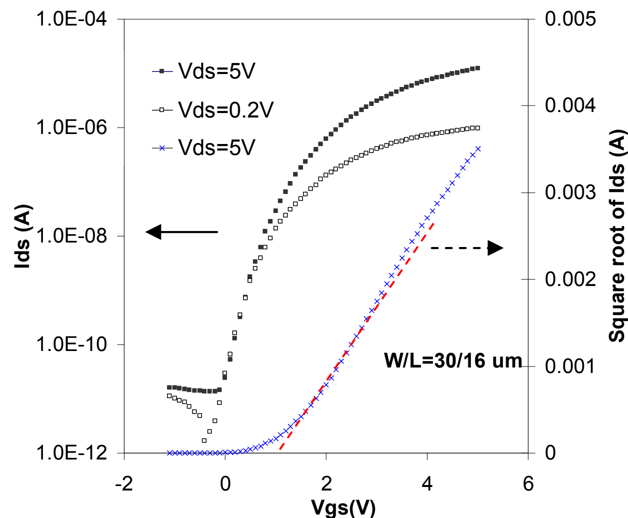
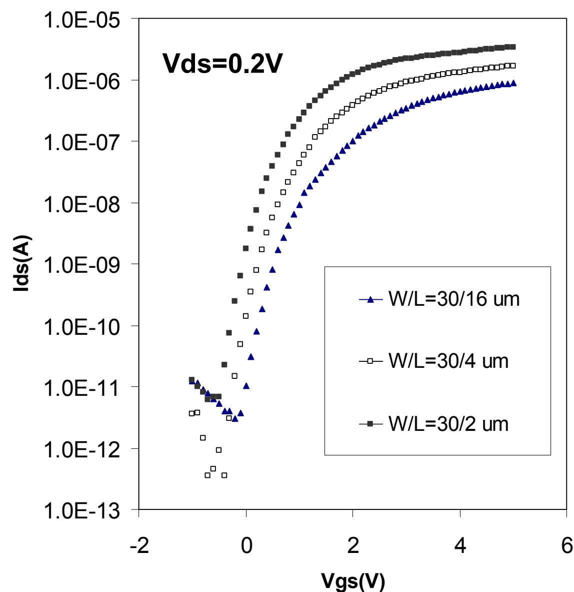
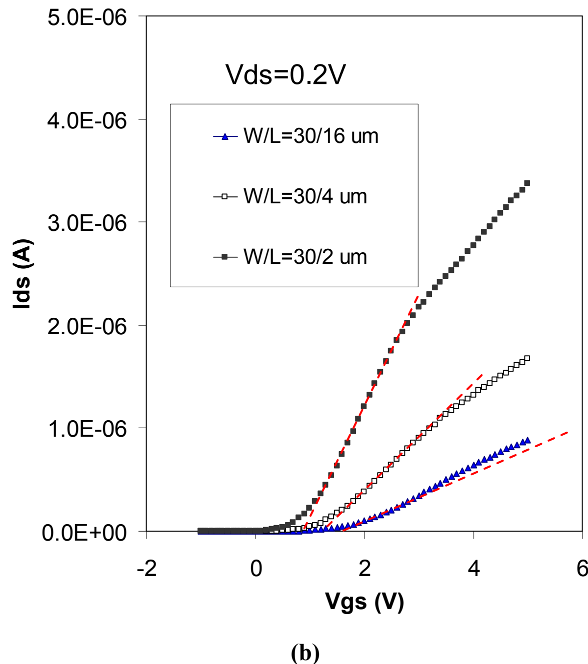


Figure 3. Transfer characteristic of ZnO TFT for V_{ds}=0.2V and 5V, respectively.

To further study the short channel effects, the transfer characteristic (at V_{ds}=0.2V) of the ZnO TFT with different channel lengths (*L*=16, 4, 2 µm) are compared in Figure 4.



(a)



(b)

Figure 4. Transfer characteristics of ZnO TFTs with the same width *W*=30 µm but different lengths *L*=16, 4, 2 µm: (a) logarithmic scale, and (b) linear scale.

From figure 4, it is seen that even the shortest channel device (L=2 µm) can be switched off by swinging gate voltage V_{gs}. It is therefore concluded that good short channel characteristics are obtained with a small shift of the threshold voltages and no degradation of subthreshold swing. This characteristic is much better than that reported earlier for devices with an inverted staggered, bottom-gate structure [10].

4. Conclusions

A novel Al_2O_3/SiO_2 gate insulator structure is developed for realizing a high performance self-aligned top-gate ZnO thin film transistors due to the efficient suppression of charge trapping at the interface between the channel layer and gate dielectrics. The ZnO TFT has a field effect mobility of 27 cm^2/Vs, a threshold voltage of 1.2 V, a subthreshold swing of 0.25 V/decade and an on/off current ratio of 10^6 at a drain voltage of 5 V. With scaling down the channel length, good characteristics are also obtained with a small shift of the threshold voltages and no degradation of subthreshold swing. The proposed top-gate ZnO TFTs in this paper can act as driving devices in the next generation flat panel displays.

5. Acknowledgements

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6. References

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