

Metal-Induced Continuous Zonal Domain (CZD) Polycrystalline Silicon Thin-Film Transistors and Its Application on Field Sequential Color Liquid Crystal Display

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Abstract—Metal induced polycrystalline silicon (poly-Si) films composing of continuous zonal domain (CZD) have been obtained through pre-defined crystalline nucleation lines (CNL). The crystallization process is precisely controllable and repeatable. P-channel thin-film transistors (TFTs) built on CZD poly-Si present high performance and high uniformity. Based on this CZD poly-Si TFT technology, which provides fast addressing characteristics and a large aperture ratio, together with a fast liquid crystal mode, a field sequential color liquid crystal display (FSC-LCD) prototype is designed and fabricated successfully. Excellent color purity and fast moving image can be obtained.

Index Terms—Active matrix LCD, field sequential color (FSC), metal-induced crystallization, polycrystalline silicon (poly-Si) thin-film transistor (poly-Si TFT).

I. INTRODUCTION

THIN-FILM transistors (TFTs) are essential for high resolution flat-panel displays [1], [2]. Liquid crystal displays (LCDs) are dominant among all the flat panel technologies. TFT-LCD technology has a wide range of applications, ranging from small consumer products such as cell phones, digital still cameras to larger displays such as desktop computer monitors and televisions [3]. TFT LCD has a huge mature manufacturing base [4]. High optical efficiency, and low cost are becoming the critical factors for LCD displays, especially for portable applications [5], [6].

For color filter (CF) based LCD, red, green and blue (RGB) sub-pixels are needed as shown in Fig. 1(a). In this arrangement, high optical efficiency and high color purity cannot co-exist [7], [8]. High color purity often needs thicker CF and hence poorer optical transparency [9], [10]. Even if color purity is compromised, CF-based display still suffers from poor optical efficiency. Even in the best case, less than 10% of the backlight can be utilized.

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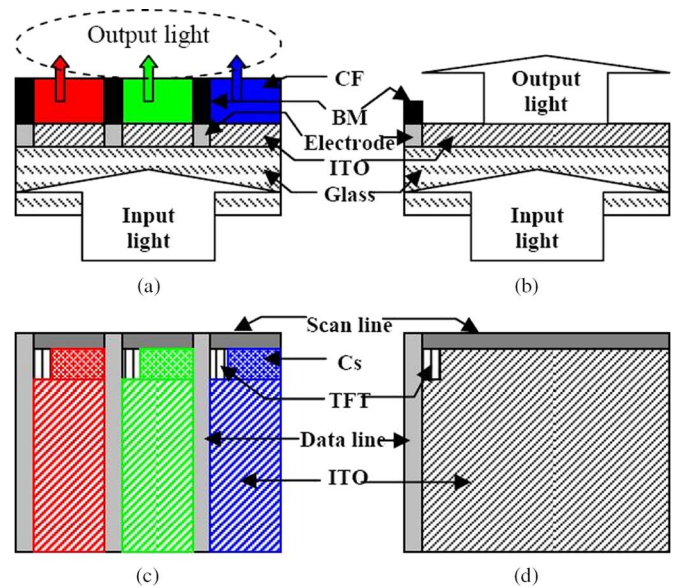


Fig. 1. Schematic cross section for (a) traditional color filter LCD, (b) field sequential color LCD, (c) pixel layout of traditional color filter LCD and (d) pixel layout for field sequential color LCD.

A field sequential color (FSC) LCD reproduces R, G, and B colors in a single pixel in a time sequential manner using synchronously pulsed colored light-emitting diodes (LED) backlights [11], [12]. The pixel structure is shown in Fig. 1(b). This method can produce a bright display with good optical efficiency since there is no CF to absorb the backlight. Moreover number of pixels of the FSC display is only one third of that of a CF display. As a result, a FSC-LCD is expected to have a higher aperture ratio (AR) than a CF display with the same resolution, thus making the optical efficiency even higher. Alternatively the same aperture ratio can be used with three times higher resolution using the same technology [13], [14].

Thus FSC-LCD is an important green technology. An important issue of FSC-LCD is color breakup artifact. To avoid color breakup, a higher frame rate such as 90 Hz instead of 60 Hz is needed. Thus the sub-frame rate is 270 Hz with a frame period of only 3.7 ms. Thus to realize FSC, a fast LCD mode together with fast electronic addressing of the TFT panel are needed. It is believed that polycrystalline silicon (poly-Si) TFT with much higher mobility is needed for fast data loading on the TFT panel. The detailed calculation results will be shown in Section II. In

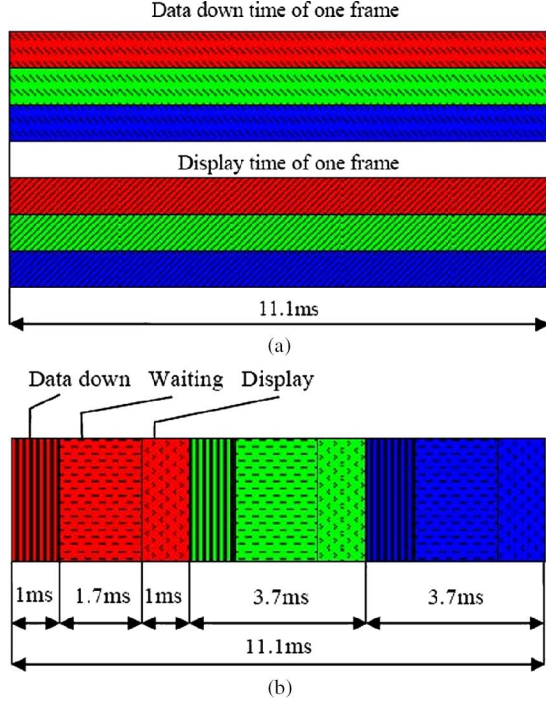


Fig. 2. Driving principle of (a) color-filter LCD and (b) FSC-LCD.

this paper, we shall discuss a fast addressing TFT using continuous zonal domain (CZD) poly-Si technology. It will be shown that fast loading is possible to realize a high quality FSC-LCD.

II. DESIGN OF THE ACTIVE MATRIX ARRAY

A. The Principle of FSC-LCD

The working principle of a field sequential color LCD is to display the red, green and blue (RGB) sub-frames of a display time sequentially. Visual color mixing will yield a full color display if the frame rate is fast enough. The RGB sub-frames can be achieved by using independently controlled RGB LED backlight. By controlling the gray-level of sub-frames, a full color display can be obtained, with a color saturation which is usually better than color filter (CF) type displays.

The sub-frame rate of FSC-LCD should be three times as fast as a conventional CF LCD, assuming the same frame rate. However, in order to reduce color breakup artifacts, even higher sub-frame rate should be employed. The principle of the driving for FSC-LCD is shown in Fig. 2(b). For a QVGA display with 90 Hz frame rate, one frame should have a duration of approximate 11.1 ms. The duration of each sub-frame is therefore only 3.7 ms. Assuming a fast response time for the LCD of 1.7 ms and the minimum LED illumination duty cycle of 30%, only around 1 ms is left for data loading, as shown in Fig. 2(b). For a color-filter LCD with the same resolution, the data loading, LCD response and LED illumination can occur at same time, as shown in Fig. 2(a). That means the loading time for FSC-LCD is one tenth of that for color filter LCD assuming the same resolution. Thus fast data loading is a key issue for FSC-LCD. That is the main theme of this paper.

B. Design of the TFT

First we analyze what is required of the pixel TFT in AM FSC-LCD. With V_D representing the voltage on the data line, the voltage level on the pixel as a function of time (t) is approximately described by the following equations:

$$V_{\text{write}} = V_D \left(1 - e^{-\frac{t}{\tau_{\text{on}}}}\right); \quad \tau_{\text{on}} = R_{\text{on}} C_s \quad (1)$$

when selected, and

$$V_{\text{hold}} = V_D e^{-\frac{t}{\tau_{\text{off}}}}; \quad \tau_{\text{off}} = R_{\text{off}} C_s. \quad (2)$$

when not selected.

R_{on} and R_{off} are the resistance of the pixel TFT at the “on” and “off” states, respectively. V_{write} and V_{hold} are the voltage on the pixel electrode during charging process and holding process.

When writing images to the LC, it is required that

$$V_{\text{write}} \succ 0.99V_D \Rightarrow T_{\text{writing}} \succ 4.6\tau_{\text{on}}. \quad (3)$$

In the images holding process, it is required that

$$V_{\text{hold}} \succ 0.95V_D \Rightarrow T_{\text{holding}} \prec \frac{\tau_{\text{off}}}{19.5}. \quad (4)$$

Therefore

$$\tau_{\text{on}} \prec \frac{T_{\text{writing}}}{4.6} \Rightarrow R_{\text{on}} \prec \frac{T_{\text{writing}}}{4.6C_s} \quad (5)$$

$$\tau_{\text{off}} \succ 19.5T_{\text{holding}} \Rightarrow R_{\text{off}} \succ \frac{19.5T_{\text{holding}}}{C_s} \quad (6)$$

where T_{writing} is the time of writing the image and T_{holding} is the time of holding the image, this is a typical frame period in display standard. In the AM FSC-LCD display, C_s is ~ 1.0 pF in the present design. As mentioned before, the time limit for each sub-frame is only 3.7 ms. So the holding time is 3.7 ms, R_{off} should be $R_{\text{off}} \succ 19.5T_{\text{holding}}/C_s = 7.2 \times 10^{10} \Omega$.

The FSC-LCD should be driven three times as fast as a conventional LCD assuming the same frame rate. The time for data loading for one frame is only about 1 ms, so it requires much smaller R_{on} than the conventional LCD. For the address TFT, it works in the linear region, the drain current (I_d) is given by

$$I_{\text{ds}} = \mu_{FE} \frac{\varepsilon_0 \varepsilon}{t_{\text{ox}}} \times \frac{W}{L} \times (V_{\text{gs}} - V_T) \times V_D \quad (7)$$

$$\Rightarrow R_{\text{on}} = \frac{V_D}{I_{\text{ds}}} = \frac{t_{\text{ox}} L}{\mu_{FE} \varepsilon_0 \varepsilon W (V_{\text{gs}} - V_T)} \quad (8)$$

where μ_{FE} is the field-effect mobility, $\varepsilon_0 \varepsilon$ is the dielectric constant of gate oxide, W and L are the effective width and length of the TFT, V_{gs} is the applied gate to source voltage and V_T is the threshold voltage. Combine with the (5), the ratio of width to length (W/L) of TFT can be written as

$$\frac{W}{L} \succ \frac{4.6 \times C_s t_{\text{ox}}}{\mu_{FE} \varepsilon_0 \varepsilon (V_{\text{gs}} - V_T) \times T_{\text{writing}}} \quad (9)$$

Here, we assume at “on” state, V_{gs} of the TFT is 15 V and $C_s = 1.0$ pF. With the parameters of the a-Si:H TFT and Poly-Si TFT listed in Table I, the required ratio of channel width (W) to length (L) of the TFT can be derived with (9), as listed

TABLE I
TYPICAL PARAMETERS OF POLY-Si TFT AND a-Si:H TFT

	μ_{Max} (cm^2/Vs)	μ_{Work} point (cm^2/Vs)	Gate Insulator	T_{ox} (nm)	ϵ
a-Si:H TFT	0.8	0.4	SiN _x	300	7.0
Poly-Si TFT	60	30	LTO	50	4.0

TABLE II
RATIO OF WIDTH TO LENGTH OF ADDRESSING TFT

Resolution	Rows (lines)	T_{writing} (μs)	W/L (a-Si:H TFT)	W/L (Poly-Si TFT)
QVGA	240	4.0	14	0.06 (0.5 or 1)
VGA	480	2.0	28	0.12 (0.5 or 1)
XGA	768	1.3	47	0.24 (0.5 or 1)
SXGA	1024	0.9	60	0.3 (0.5 or 1)

in Table II. For a QVGA display with 90 Hz frame rate, the writing time is 4 μs for every pixel. The ratio of W/L of a-Si:H TFT requires at least 14. At the same time, the ratio of W/L of Poly-Si TFT requires only 0.06. It means for the 5 μm process, the width of the TFT channel is 70 μm for a-Si:H TFT and 0.3 μm for poly-Si TFT theoretically. For higher resolution display, the writing time for every pixel decreases, so the TFT with larger W/L ratio is required. Taking SXGA display for example, the limited writing time is only 0.9 μs . The channel width of a-Si:H TFT requires at least 300 μm based on 5 μm process that is totally impossible for high definition display. Compared to a-Si:H TFT, higher aperture ratio (AR) can be reached using poly-Si TFT due to the higher field effect mobility.

Here, assuming the pixel size is fixed at 200 $\mu\text{m} \times 200 \mu\text{m}$, the width of both scan line and data line is 12 μm . The minimum space at same layer is 5 μm , and the minimum space for different layer is 2 μm . Normally, the gate length of TFT is 5 μm or 10 μm in LCD display. Based on these process parameters the typical layout for a pixel, which has only one TFT, the ratio of W/L of TFT for different resolution employing a-Si:H TFT and poly-Si TFT are listed in Table II. As we know, for reality, the photolithography process is unable to provide a line width or length smaller than the technology feature ($2\lambda = 5 \mu\text{m}$), which means the W and L of TFT could not be smaller than 2λ . For example, if $L = 5 \mu\text{m}$, W of TFT has to be larger than 5 μm , which means W/L must be equal or larger than 1. If $L = 10 \mu\text{m}$, W of TFT has to be larger than 5 μm , which means W/L must be equal or larger than 0.5. So, in Table II, for poly-Si TFT, all the W/L of TFT was set to 0.5 and 1 for aperture ratio (AR) calculation for $L = 5 \mu\text{m}$ and $L = 10 \mu\text{m}$ respectively. Fig. 3 shows the AR as a function of the number of scan line using a-Si:H TFT and poly-Si TFT as addressing TFT based on 5 and 10 μm TFT gate length, respectively. For the a-Si:H TFT, the AR of pixel decreases with the increasing of scan lines. For poly-Si TFT, the AR of pixel almost maintains at 77%–78% due to the constant value of W/L . So poly-Si TFT is necessary for achieving high resolution and high AR display.

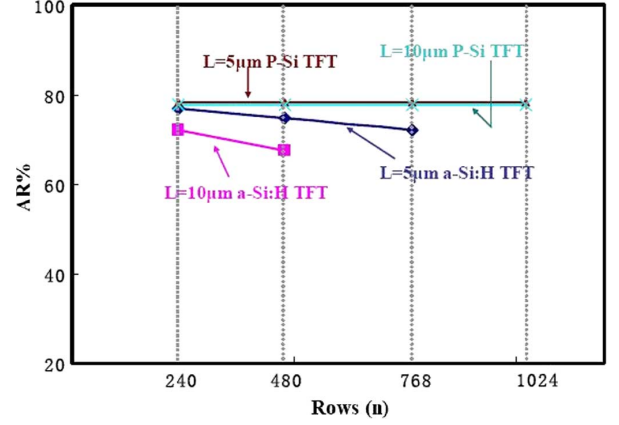


Fig. 3. AR as a function of the number of scan lines using a-Si:H TFT and poly-Si TFT. based on 5 and 10 μm process, respectively.

III. POLY-Si TECHNOLOGY

A. Poly-Si TFT Introduction

Low temperature crystallization of amorphous silicon (a-Si) thin film has attracted considerable attention because of its potential applications to large area electronics on inexpensive glass substrates and its high mobility. TFTs, built on metal-induced lateral crystallized (MILC) polycrystalline silicon (poly-Si), have shown high carrier mobility and good device uniformity. They can be used to realize active-matrices for flat-panel display and image sensor applications [15].

However, traditional MILC-TFTs [16] have problems of subsequent mask misalignment induced by glass substrate shrinking during the crystallization process. Additionally, residual nickel in the poly-Si channel affects the long term stability of the TFTs.

There have been several attempts to reduce the Ni content in MIC based TFT. Giant grain silicon (GGS) has been obtained by Ni-mediated crystallization of a-Si with a silicon-nitride (SiN_x) cap layer [17] or using solution based metal-induced crystallization (SMIC) [18]. The problem of subsequent mask misalignment induced by glass substrate shrinking can be solved with these technology, but the random distribution of crystalline nuclei leads to longer annealing time, which is not acceptable for large area glass substrate.

A new implementation scheme which can reduce residual nickel in poly-Si as well as annealing time is proposed and demonstrated. The nickel content and distribution in crystallized continuous zonal domain (CZD) poly-Si film is analyzed by time of flight Secondary Ion Mass Spectrometry (ToF-SIMS). P-channel TFTs built on this CZD poly-Si exhibit high performance and high uniformity.

B. CZD Material Formation and Analysis

1) *CZD Material Formation*: The fabrication process began with the deposition of 300-nm silicon oxide (SiO₂) using plasma-enhanced chemical vapor deposition (PEVCD) on Eagle 2000 glass substrate. Then 45 nm a-Si was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Subsequently, a SiO₂ nano-cover layer was formed on the surface of a-Si. After that, a layer of photoresist (PR)

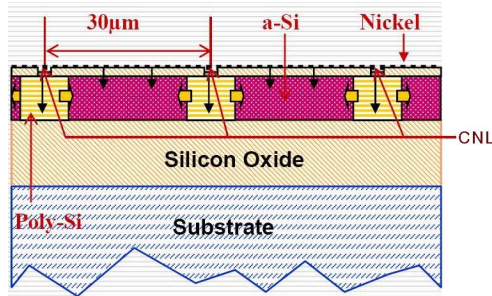


Fig. 4. Cross section of the CZD structure.

was spin-coated on surface and it was defined as uniformly distributed lines in width of $1.5 \mu\text{m}$ and space of $30 \mu\text{m}$ from the neighboring lines. The length of the line is equal to the width of the substrate. The SiO_2 nano-cover layer was etched using 777 etchant with PR as a mask. After etching, the PR was removed by a mixed solution of H_2SO_4 and H_2O_2 at 120°C . At the same time a $\sim 2\text{-nm}$ layer chemical oxide was formed on a-Si surface where SiO_2 nano-cover layer was removed by 777. Then an ultra-thin layer of nickel was sputtered on the surface of this structure. The schematic of the CZD structure was shown in Fig. 4. After annealing at 590°C for 1 hour the a-Si was fully crystallized. The width of the zonal domains was half of the distance between two neighboring crystalline nucleation lines (CNL), and the length of the zonal domains was the same as the width of the substrate, which can be tens of centimeters to several meters.

2) *Comparison With GGS Poly-Si:* The metal-induced poly-Si films composed of CZD in exactly same width can be obtained through pre-defining CNL on a nano-layer of silicon dioxide. After the crystallization process, the entire poly-Si film can be the active layer of high performance TFTs, so the impact of glass substrate shrinking on subsequent alignment process is eliminated. All CZDs have exactly the same width and length so that the crystallization process is strictly controllable and the annealing time is shorter than one hour at 590°C . Fig. 5 shows the optical microscopy images of poly-Si films after one hour annealing at 590°C in nitrogen (N_2) atmosphere using GGS and CZD technology respectively. The films are etched by tetra-methyl ammonium hydroxide (TMAH) for better inspection. As shown in Fig. 5 the CZD film has been fully crystallized and the GGS film still has a lot of areas not crystallized. Fig. 6 shows the average crystallization fraction over large area substrate of the film employing GGS and CZD technology as a function of the annealing time at 590°C . 100% crystallization fraction can be obtained using CZD technology at 60 min, while that is just about 50% for the GGS technology.

3) *Comparison With MILC Poly-Si:* To compare the residual nickel concentration in CZD and metal induced lateral crystallization (MILC) poly-Si films after the crystallization process, the Ni content and distribution in CZD and MILC poly-Si films were measured by time of flight Secondary Ion Mass Spectrometry (ToF-SIMS). The nickel content in CZD film is two orders of magnitude lower than that in MILC film [Fig. 7(a)]. Fig. 7(b) and (c) show the two-dimensional (2D) distribution of Ni in MILC and CZD poly-Si films, respectively. Nickel and/or

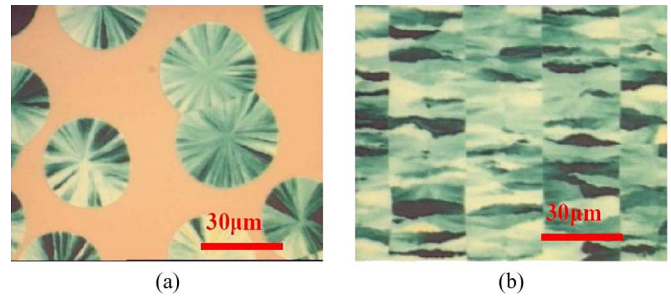


Fig. 5. Optical microscopy images of amorphous silicon film after one hour annealing at 590°C in N_2 atmosphere employing (a) GGS technology and (b) CZD technology.

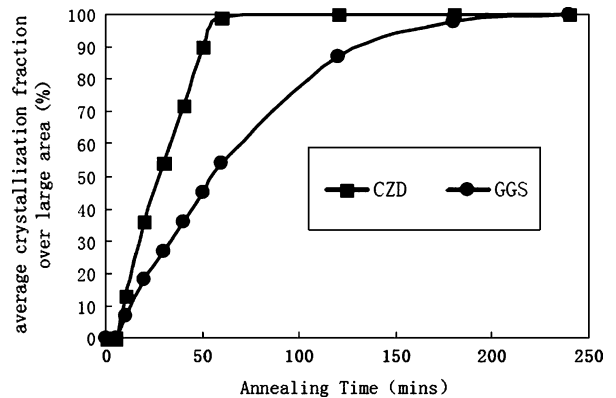


Fig. 6. The average crystallization fraction over large area using CZD and GGS technology versus the annealing time at 590°C .

nickel silicide are denoted as bright dots in the 2D images. In 2D image of MILC poly-Si film [Fig. 7(b)], the bright columns on both sides are MIC regions and the dim line in the middle is the intersection of two MILC regions. It reveals that the nickel content is a little higher at the intersection and much higher in the MIC regions.

In the 2D image of CZD poly-Si film [Fig. 7(c)], similar to the MIC region of MILC films, a higher Ni concentration is distributed at the crystalline nuclei lines region (CNL). But the ratio of MIC region to MILC region in MILC films was much higher than that of CNL region to lateral region in CZD films. It means that there is no area on the CZD poly-Si which contains a very high concentration of Ni. The entire poly-Si film is available for the active layer in TFT. So it means that the CZD poly-Si films have lower Ni concentration and higher uniformity.

IV. ACTIVE MATRIX FABRICATION AND RESULTS

A. Fabrication for Active Matrix

The CZD poly-Si film was patterned into active islands by wet etching with Freckle etchant. 50 nm low temperature oxide (LTO) was subsequently deposited by LPCVD at 425°C as the gate insulator. Following defining gate electrodes and the scan line, boron at a dose of $4 \times 10^{15}/\text{cm}^2$ was implanted into the source and drain. A 600-nm PECVD oxide as isolation layer was deposited and contact holes were opened. Subsequently, 700-nm aluminum-1%Si was sputtered and patterned to form the inter-connections. Contact sintering was then performed in

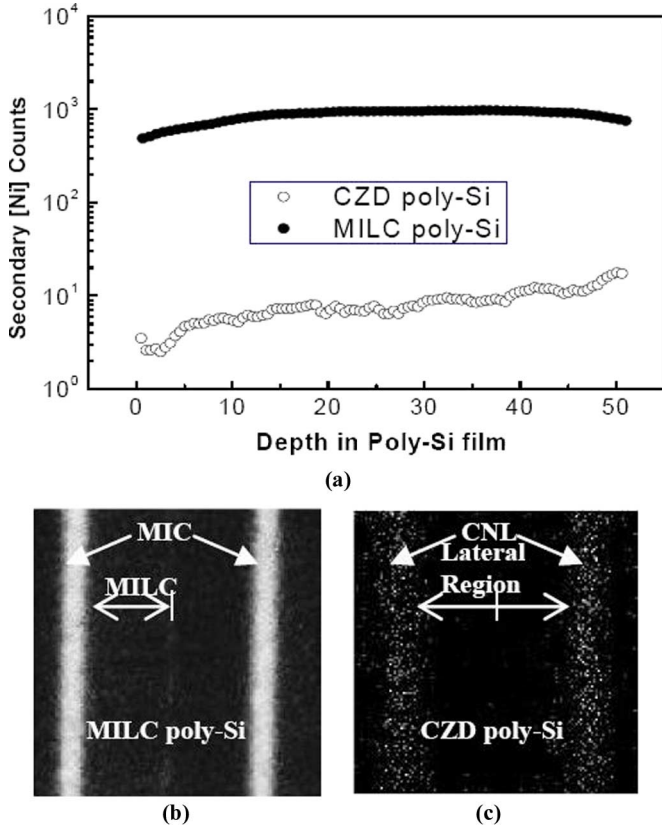


Fig. 7. SIMS depth profiles of nickel content (a) and 2-D image of Ni distribution in (b) MILC poly-Si film and (c) CZD poly-Si film traced by SIMS.

forming gas at 420 °C for 30 min and the dopants were activated at the same time. The pixel electrode indium thin oxide (ITO) was patterned by lift-off process. Finally the black matrix was defined to reduce the reflection of Al electrode. The panel was the ready for LCD integration.

W/L of our TFT is 24 $\mu\text{m}/5 \mu\text{m} \times 2$, which is different from the calculation results of 5 $\mu\text{m}/5 \mu\text{m}$. 2 separate gates structure is used to reduce the leakage current of CZD poly-Si TFT. A larger W/L was used to increase the “on” state current and reduce the writing time for every pixel, on the premise of not decreasing the aperture ratio of display panel by 1% based on the pixel structure mentioned before.

Electrical characteristics of CZD poly-Si TFTs were measured with HP4156 semiconductor parameter analyzer. Transfer characteristic curves and their field effect mobility (μ_{FE}) of TFTs are shown in Fig. 8. The threshold voltage (V_{th}) is defined as the V_g required to induce an $I_d = W/L \times 10^{-7}$ A at $V_{\text{ds}} = -5$ V. The field-effect mobility (μ_{FE}) at low drain voltage is given by

$$\mu_{\text{FE}} = \frac{Lg_m}{WC_{\text{ox}}V_{\text{ds}}}$$

where W and L are the effective channel width and length, g_m is the transconductance, C_{ox} is the gate insulator capacitance per unit area, V_{ds} is the voltage between drain and source. The reported field-effect mobility is the maximum value measured.

The p-channel CZD poly-Si TFTs exhibited a maximum field effect mobility (μ_{FE}) of 65 $\text{cm}^2/\text{V} \cdot \text{s}$. The subthreshold swing

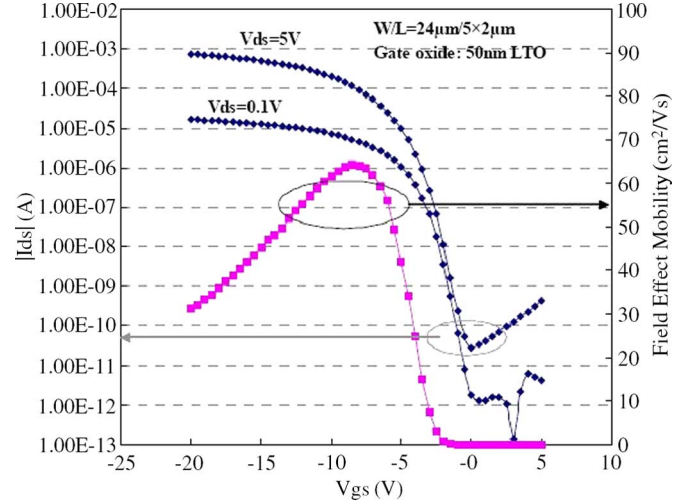


Fig. 8. Transfer characteristic curves and their field-effect mobility (μ_{FE}) for TFTs.

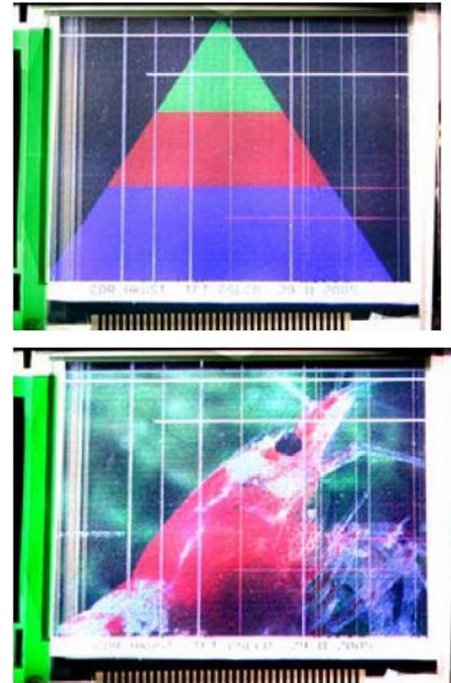


Fig. 9. Representative image from the 3-in QVGA active matrix FSC-LCD prototype.

(S) was 0.56 V/dec and the threshold voltage (V_{th}) was -3.6 V. The on state current and off state current of the TFTs are 7.36×10^{-4} A and 4.1×10^{-11} A respectively. The ratio of on-state to off-state drain current is 2.6×10^7 . These are typical numbers from our experiment. Compared to literature values, they are quite good.

This active matrix backplane was used to fabricate an LCD. As mentioned before, the LCD mode has to be very fast for FSC applications. A transient mode based on optical rebound was employed [19]. This mode has previously been used for making a passively driven FSC display. It relies on the optical bounce which is a transient effect [20]. Thus it overcomes the difficult requirement of having to use a very fast LCD mode. Details

of the operation and principle of this LCD has been discussed before [20]. Essentially it is noted that with a sub-frame time of only 3.7 ms (sub-frame frequency is 90×3 Hz), it is very difficult to have a transition from one stable LC alignment to another LC alignment. However, the transient can occur very fast. All the grey level can be obtained within 1.8 ms when LC cell gap is $5 \mu\text{m}$. The driving voltage is also very low <4 V. Since in FSC, the LED is on for a very short time (1 ms) it is in fact not necessary for the LC alignment to be a stable state. A transient state works perfectly. Fig. 9 shows the representative image from this 3-in QVGA active matrix FSC-LCD.

V. CONCLUSION

In this paper, we presented data and design criteria for a 3-in QVGA active matrix backplane for FSC-LCD. It was noted that in order for fast data loading, LTPS TFT is needed. The fabrication of this backplane using the technology of metal-induced CZD poly-Si TFTS was presented. The display realizes good colors in a video display. A prototype FSC LCD was constructed using a transient LCD mode. It worked well showing vivid colors in a field sequential manner.

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