59.3: Bridged-grain (BG) Eximer Laser Annealing (ELA) Polycrystalline Silicon Thin Film Transistors (TFTs)

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Abstract:
A new technique bridged-grain (BG) was introduced. Using this BG eximer laser annealing (ELA) poly-Si as an active layer, the grain boundary effects can be reduced. Important electrical properties such as sub-threshold swing, threshold voltage, maximum field effect mobility, leakage current, on-off ratio and device uniformity across the substrate can all be improved using the present technique. The improvement can be achieved at low cost, thus making inexpensive, high performance LTPS TFT a reality.

1. Introduction:

Among existing display technologies, active-matrix organic light emitting diodes (AMOLEDs) is regarded as the best candidate for an 'ultimate display' due to their superior characteristics, such as self-emission, fast motion picture response, vivid colors, wide view angle, high contrast, and super-slim [1, 2]. Low temperature poly silicon (LTPS) thin film transistors (TFTs) attracted more and more attention due to their superb current-driving capability and electrical reliability. It is well known that the LTPS has the potential for peripheral circuits to realize system on panel (SOP) due to the higher mobility than a-Si TFTs. To reduce the manufacture cost and mask number, a lot of PMOS circuit for display have been proposed, including shift registers, level shifters, demultiplexers, and DC-DC converter [3]. Thus low cost, high performance and reliable LTPS processing technologies are greatly required [4]. Considering the trade-off between performance and economic issue, three kinds of LTPS technology survived out of multifarious approaches, each with its own advantages and disadvantages. They are solid phase crystallization (SPC) [5], excimer laser annealing (ELA) [6] and metal induced crystallization [7].

Among these methods, ELA has been the most widely used due to its excellent crystallization quality, fast crystallization speed, and high mobility. In 2004, 2 inch System on Glass (SOG) QVGA (240×320) TFT-LCD with integrated 6-bit source driver circuit was fabricated employing the high-performance Two-Shot Sequential Lateral Solidification (TS-SLS) TFTs [8]. In 2008 SID, Samsung demonstrated 14 inch WXGA AMOLED with SLS base TFT backplane [9]. They already had some products in mobile display, such as i9000 Galaxy S with a 4 inch 480×800 LTPS-AMOLED panel.

Even ELA is already employed in mass-production, the ELA poly-Si TFT still suffers from the non-uniformity of TFT current output due to its differences in threshold voltage, mobility and sub-threshold swing from different degree of crystallization of TFTs. The non-uniform brightness from pixel to pixel was observed. In addition, one of the important problems of ELA-TFTs is large off-state current. An important approach for reducing leakage current is to decrease the electric field in the drain depletion region, normally it was achieved by replacing poly-Si TFTs with a self-aligned structure by those with a lighted doped drain (LDD) structure.

In this paper, we proposed a new method to improve the properties of ELA TFTs. Using bridged-grain (BG) ELA poly-Si as an active layer, the grain boundary effects can be reduced. Important properties such as threshold voltage, on-off ratio, device mobility, device uniformity across the substrate, sub-threshold slope and device reliability, can all be improved using the present technique. The improvement can be achieved at low cost, thus making inexpensive, high performance LTPS TFT a reality.

2. Fabrication of ELA+BG poly-Si TFT

These BG-ELA poly-Si films were patterned into active islands by dry etching with AME8110 reactive ion etcher. After dry etching, photoresist was removed by O_2 plasma. 100nm low temperature oxide (LTO) was subsequently deposited by LPCVD at 425°C as the gate insulator after the native oxide was removed by 1% HF. Following the deposition of 300nm Titanium which was patterned into gate electrodes, boron and phosphor at a dose of $4\times10^{15}/cm^2$ was implanted into the S/D for p-channel TFT and n-channel TFT, respectively. A 500nm LTO isolation layer was deposited. Contact holes were opened before 700nm aluminum-1%Si was sputtered and patterned as contacts. Contact sintering was then performed in forming gas (FGA) at 420°C for 30mins.

3. Device characterization and discussion

Electrical characteristics of both p-channel and n-channel TFTs built on 45nm ELA and ELA+BG poly-Si were measured with HP4156 semiconductor parameter analyzer.

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Firstly, transfer characteristic curves for TFTs of which W/L was 30μm/10μm were tested. W and L denote the channel width and gate length of the transistor respectively, as shown in Figure 1. The threshold voltage (V_{th}) defined as the V_g required to induce an I_d of W/L×10^{-7} A at $|V_{ds}|$=5V.

The field-effect mobility (μ_{FE}) of normal ELA TFT at low drain voltage is given by

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{ds}} \qquad (1)$$

Where g_m is the transconductance, C_{ox} is the gate insulator capacitance per unit area, V_{ds} is the voltage between drain and source. The reported field-effect mobility is the maximum value measured.

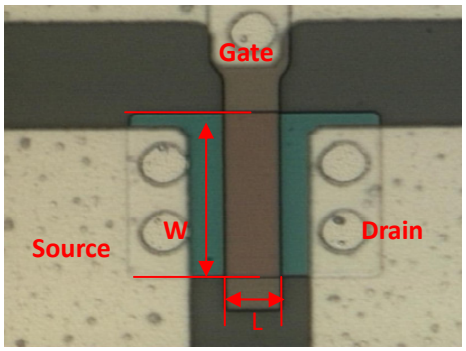

Figure 1. Microscope photo of the TFT.

Figure 2 shows the transfer characteristics of p-channel ELA and BG-ELA TFTs when Vds=-0.1V and Vds=-5V. Figure 3 shows the transfer characteristics of n-channel ELA and BG-ELA TFTs when Vds=0.1V and Vds=5V.The important electrical parameters of BG-ELA and ELA TFTs are listed in Table 1, including both p- and n-channel TFTs.

The effective channel length of BG-TFT is changed due to the BG structure. To better investigate the BG effects, the IV curves of BG-ELA TFTs are needs to be processed according to the channel length modulation by BG structure. Here, we assume that, the field effect mobility of ELA-poly-Si at "on" state remains unchanged whether there is BG or not. When the TFT are working at "on" state. When Vds=-5V, the "on" state current of normal p-channel ELA TFT with BG and without BG is 1.35×10^{-3} A and 7.56×10^{-4}A respctviely. The current ratios between p-channel TFTs with BG and without BG is 1.78. The designed channel width and length for TFTs are 30μm and 10μm, respectively. So, the effective channel length of ELA TFTs with BG is the length of gate to be devided by the factor of 1.78. As a result, the effective channel length of BG-ELA TFTs for p-channel and n-channel are 5.62μm and 4.59μm, respectively. As shown in table 1, the maximum field effect mobility of TFTs with BG structure are increased by 30%.

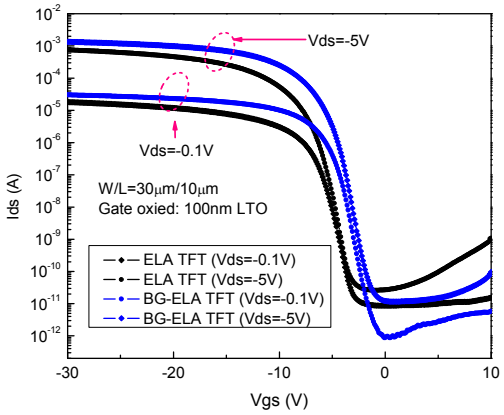

Figure 2. The transconductive curves of p-channel BG-ELA and ELA TFTs, when Vds=-0.1V and Vds=-5V.

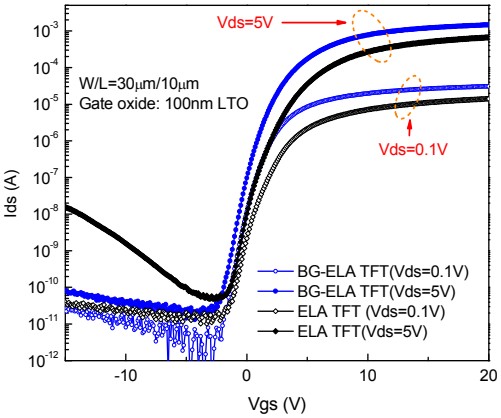

Figure 3. The transconductive curves of n-channel BG-ELA and ELA TFTs, when Vds=0.1V and Vds=5V.

Table 1. Key device parameters of BG-ELA and normal ELA TFTs, including both n-channel and p-channel.

	P-Channel		N-Channel	
	ELA	BG+ ELA	ELA	BG+ ELA
μ_{FE}(cm^2/Vs)	101	139	105	134
V_{th} (V)	-6	-4	1.3	0.4
S (V/decade)	0.72	0.6	0.734	0.64
I_{off} (pA/μm) Minimum	0.9	0.39	1.62	0.437
GIDL (pA/μm) $\lvert V_{ds} \rvert$=5V $\lvert V_{gs} \rvert$=10V	25	3.23	52.67	1.25
I_{on}/I_{off} (×10^7) $\lvert V_{ds} \rvert$=5V	1.78	11.25	1.37	11.1

The subthreshold swing (S) is 0.6V/dec and 0.72V/dec for p-channel ELA TFTs with BG and without BG, respectively. Also, with BG, the absolute value of threshold voltage (V_{th}) is reduced by 2V to 4V. The subthreshold swing (S) is 0.64V/dec and 0.73V/dec for n-channel ELA TFTs with BG and without BG, respectively. Also, with BG, the threshold voltage (V_{th}) is reduced by 0.9V to 0.4V. Normally, the V_{th} and S are strongly influenced by the deep trap state, associated with danling bonds [10]. In other words, we believe that the boundary height could be lowered by the BG structure, meanwhile, some of the trap states and dangling bounds could be filled or terminated by the BG structure. Extracted from Figure 4 using a model proposed by R. E. Proano [10], the respective trap state densities for the normal ELA and BG ELA TFTs are $2.07\times10^{12}/cm^2$ and $1.67\times10^{12}/cm^2$.

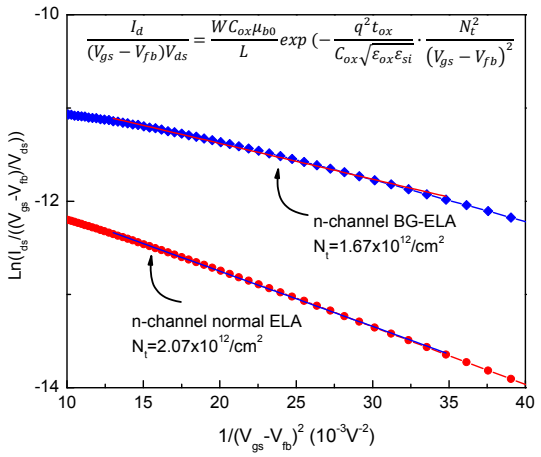

Figure 4. Plots of $\ln(I_{ds}/((V_{gs}-V_{fb})/V_{ds}))$ *vs* $1/(V_{gs}-V_{fb})^2$ for the n-type normal ELA and BG ELA TFTs

As shown in Figure 2 and Figure 3, the leakage current for both n-channel and p-channel TFTs was greatly reduced by applying BG structures to the active channel. At high V_{gs} and high V_{ds}, the leakage current is dramatically reduced by a more than one order. As a result, the on/off ratio is also greatly improved, as listed in Tabel1. When V_{gs} is smaller than V_{th}, the ELA poly-Si without implantation is intrinsic and the doped region presents N+ or P+ polarity in case of n-channel or p-channel TFTs, which means the active channel for TFTs with BG structure becomes a series of i-N+ or i-P+ shallow junctions in this case. That is why the GIDL and minimum current are both greatly decreased. From the above comparison, we can see most of the TFT parameters were dramatically improved with BG apllication.

Figure 5 (a) and (b) show the p-channel TFT performance variation, V_{th} and GIDL, for normal ELA TFTs and BG-ELA TFTs. The data was measured for 100 TFTs uniformly distributed over 4 inch glass wafers. It is clearly that the TFTs with BG structrue show much lower GIDL than normal ELA TFTs, so as to the uniformity. Meanwhile, the BG-ELA TFTs also present smaller V_{th} variation than normal ELA TFTs, as well as the absolute V_{th} value.

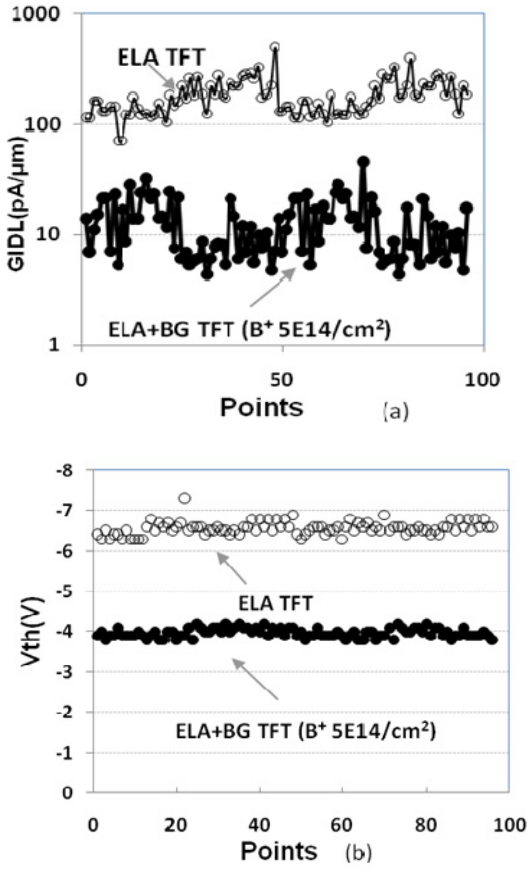

Figure 5. TFT performance variation for uniformly distributed 100 TFTs; (a) GIDL and (b) V_{th}.

4. Conclustion:

A bridged-grain (BG) technology was proposed to apply to commercial ELA TFTs. The ELA TFTs with BG structure shows smaller threshold voltage, steeper subthreshold slope, smaller leakage current, higher on-off ratio, and better device uniformity across the substrate. The improvement can be achieved at low cost, thus making inexpensive, high performance LTPS TFT a reality.

5. Acknowledgments

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