Anomalous Degradation Behavior of p-Type Polycrystalline Silicon Thin Film Transistors under Negative Gate Bias Stress

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***Abstract*-Anomalous device degradation behavior of p-type polycrystalline silicon thin film transistors under negative gate bias stress is observed. In the first stage, negative gate bias instability dominates, resulting in negative threshold voltage (V_{th}) shift while in the second stage, negative charge generation induced by hot electrons happens, giving rise to positive V_{th} shift.**

I. Introduction

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have become promising devices to achieve fully integrated active matrix displays due to the higher carrier mobility [1]. From the standpoint of fabrication technology and long term reliability, the stability of poly-Si TFTs is of significant importance. For the p-type poly-Si TFTs, negative bias temperature instability (NBTI) is found to be a key reliability issue, which results in a negative threshold voltage (V_{th}) shift under negative gate bias stress due to the generation of interface/grain boundaries (GBs) trap states and fixed oxide charge [2-4].

In this paper, degradation of p-type poly-Si TFTs under negative gate bias stress is systemically studied. It is found that when the negative gate bias exceeds certain value (−35V), TFTs exhibit anomalous degradation behavior, in which two-stage degradation happens. In the first stage, devices follow typical NBTI degradation while in the second stage V_{th} no longer negatively shifts but shifts positively. Furthermore, the turnaround point appears earlier for the higher negative gate bias stress (i.e., –40V is higher than –38V). The positive V_{th} shift is believed to be attributed to negative charge generation in the gate oxide induced by the hot carrier (HC) effect.

II. Experimental

TFTs used in this work are in conventional self-aligned top-gate structure as shown in Fig.1. First, 500-nm-thick thermal oxide was grown on 4-inch c-Si wafers in furnace. Then, 100nm a-Si active layer was deposited by low-pressure chemical vapor deposition (LPCVD). Solid phase crystallization (SPC) process was then carried out. In the SPC process, the wafer was annealed at 600ºC for 24 hours in N_2 ambient. Next 100-nm LTO layer was deposited as gate oxide, followed by sputtering of a 300nm Al as gate. After gate patterning, a self-aligned boron implantation with a dose of $4\times10^{15}cm^{-2}$ was done to form the source and the drain. The 500nm LPCVD LTO was deposited as field oxide. Contact holes were then opened before Al layer sputtering and patterning. Finally, the wafers were sintered in forming gas for 30 minutes at 450ºC.

The stress condition is also shown in Fig.1. Various negative gate bias stresses (–20V~–42V) are applied with source and drain grounded. The on-current (I_{on}) is extracted at V_g=–25V and V_{ds}=–0.1V and V_{th} is extracted from a transfer curve at V_{ds}=–0.1V using the linear extrapolation method.

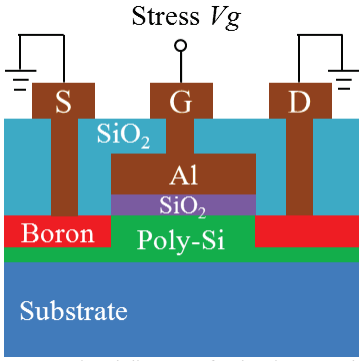

Fig.1: Schematic cross-sectional diagram of poly-Si TFT and negative gate bias stress setup.

III. Results and Discussions

Shown in Fig.2 is the transfer curve degradation of p-type poly-Si TFTs under moderate negative gate bias stress (stress V_g=–35V) measured at V_{ds}=–0.1 and –5V. Evidently, typical NBTI degradation occurs. The V_{th} continuously shifts negatively and gate-induced drain leakage (GIDL) [5] current decreases while the subthreshold slope keeps almost constant [2-4]. When the negative gate bias stress become higher (>–35V), anomalous device degradation behavior appears. As shown in Fig.3 is transfer curve degradation of p-type poly-Si TFTs under high negative gate bias stress (stress V_g=–42V) measured at V_{ds}=–0.1 and –5V. The inset is the magnification of GIDL current. It can be observed that there is a two-stage degradation. The V_{th} shifts first negatively and then positively. For the GIDL current, it first increases and then decreases. All the degradation behaviors indicate besides NBTI effect another degradation mechanism involves.

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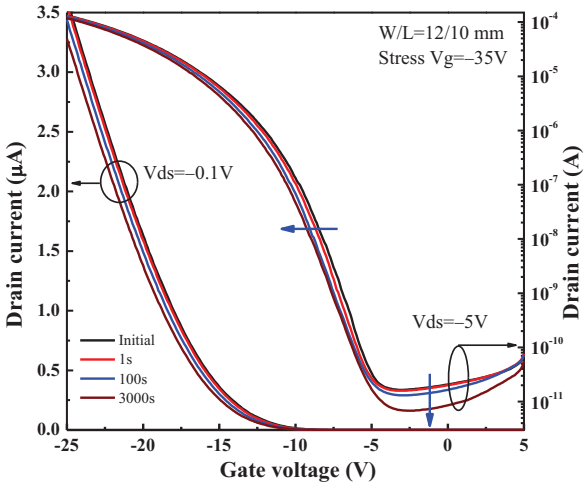

Fig.2: Typical NBTI degradation under moderate negative gate bias stress, poltted in linear and logarithmic scale.

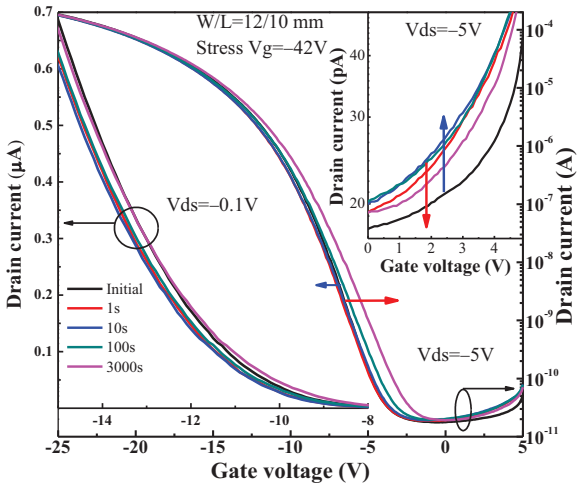

Fig.3: Anomalous degradation under high negative gate bias stress, poltted in linear and logarithmic scale.

To figure out the degradation mechanism, the amplitude effect of stress V_g is investigated as shown in Fig.4~Fig.11. Shown in Fig.4 and Fig.5 are respectively the dependence of I_{on} degradation and V_{th} shift on stress time under various moderate negative gate biases (–20V~–35V), plotted in linear scale. It can be found that NBTI degradation is enhanced by the larger amplitude of stress V_g. Shown in Fig. 6 and Fig.7 are respectively the dependence of I_{on} degradation and V_{th} shift on stress time under various moderate negative gate biases, plotted in logarithmic scale. The degradation slope of I_{on} and V_{th} are 0.28 and 0.26, which is consistent to the previous NBTI report in poly-Si TFTs [4]. Shown in Fig.8 and Fig.9 are respectively the dependence of I_{on} degradation and V_{th} shift on stress time under various high negative gate biases (–35V~–42V), plotted in linear scale. Clearly a two-stage degradation is observed. In the first stage, both I_{on} and V_{th} are degraded. Higher amplitude stress V_g brings larger I_{on} degradation and more negative V_{th} shift. After the first-stage degradation, I_{on} begins to increases and the V_{th} positively shift. Higher amplitude stress V_g brings larger I_{on} increase and more positive V_{th} shift. It is also noted that the turnaround point for both I_{on} degradation and V_{th} shift appears earlier for the higher negative gate bias stress, as indicated by the circles in Fig.8 and Fig.9. Shown in Fig. 10 and Fig.11 are respectively the dependence of I_{on} degradation and V_{th} shift on stress time under various high negative gate biases, plotted in logarithmic scale. For the first-stage degradation, the slope is consistent to the NBTI degradation slope, indicating NBTI's dominating the first-stage degradation. For the second-stage degradation, the degradation slope is strikingly different from that of NBTI, implying another degradation mechanism must involve.

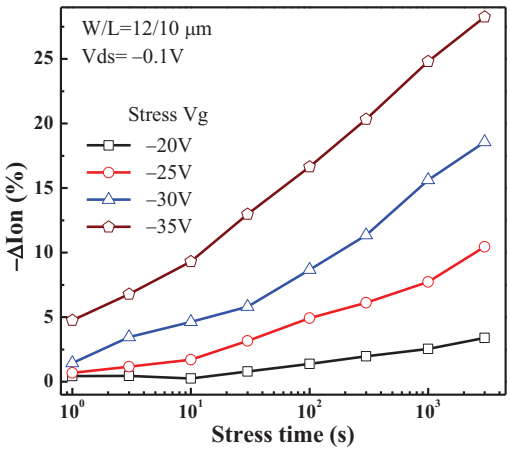

Fig.4: Dependence of I_{on} degradation on stress time under various moderate negative gate biases, plotted in linear scale.

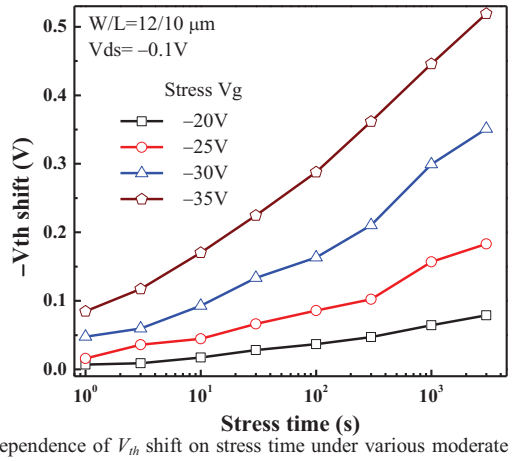

Fig.5: Dependence of V_{th} shift on stress time under various moderate negative gate biases, plotted in linear scale.

To better under this two-stage degradation mechanism, energy band diagram of p-type ploy-Si TFTs under high negative gate bias stress is presented as shown in Fig.12. In the first stage, the NBTI effect dominates, which is mainly attributed to the generation of positive fixed charges and interface/GB trap states [3]. For the second-stage degradation, it is inferred that hot electrons induced the impact ionization in the high electric field would break the bond of Si-OH at interface/GBs [3] and then, the negative ions (OH^-) are generated and diffuse into the gate oxide which positively shift the V_{th}, as shown in Fig.12.

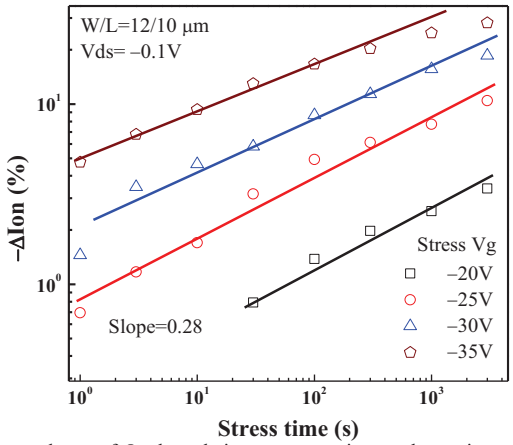

Fig.6: Dependence of I_{on} degradation on stress time under various moderate negative gate biases, plotted in logarithmic scale.

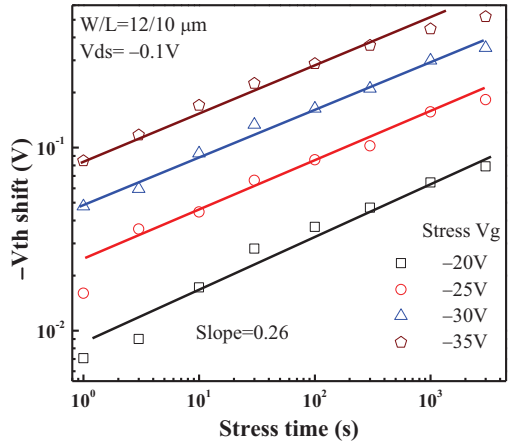

Fig.7: Dependence of V_{th} shift on stress time under various moderate negative gate biases, plotted in logarithmic scale.

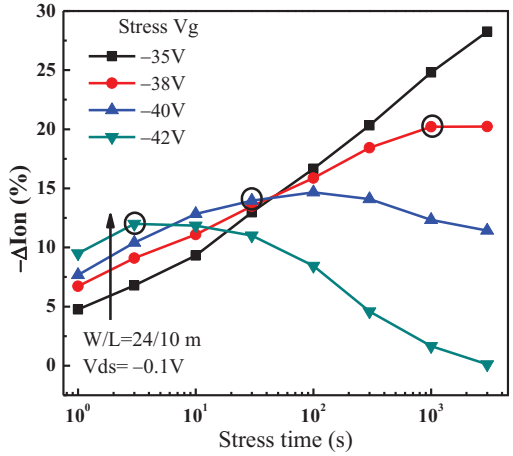

Fig.8: Dependence of I_{on} degradation on stress time under various high negative gate biases, plotted in linear scale.

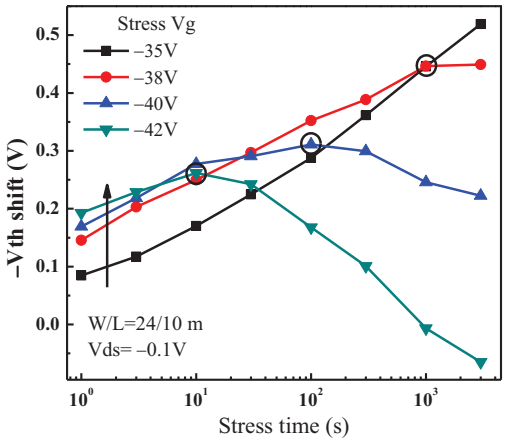

Fig.9: Dependence of V_{th} shift on stress time under various high negative gate biases, plotted in linear scale.

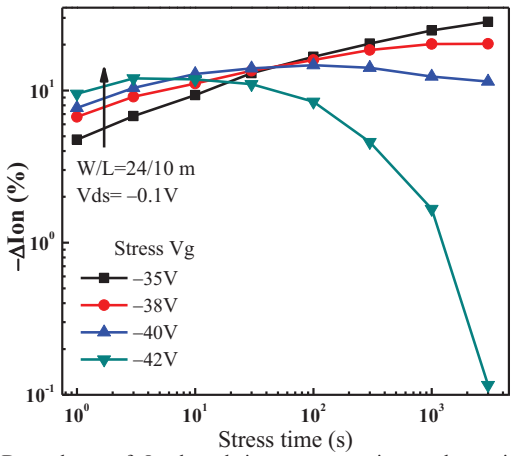

Fig.10: Dependence of I_{on} degradation on stress time under various high negative gate biases, plotted in logarithmic scale.

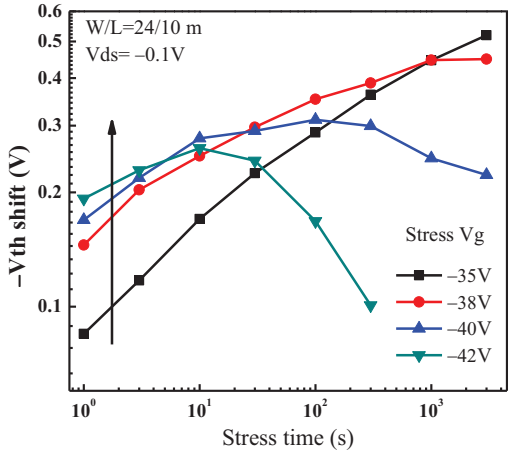

Fig.11: Dependence of V_{th} shift on stress time under various high negative gate biases, plotted in logarithmic scale.

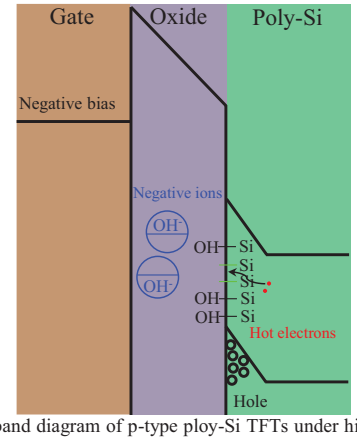

Fig.12: Energy band diagram of p-type ploy-Si TFTs under high negative gate bias stress.

IV. Summary

Device degradation of p-type poly-Si TFTs under negative gate bias stresses is systematically investigated. An Anomalous degradation behavior under high negative gate bias stresses is observed. NBTI dominates the first-stage degradation while the second-stage degradation is attributed to negative charge generation induced by hot electrons.

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