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Water-enhanced negative bias temperature instability in p-type low temperature polycrystalline silicon thin film transistors

Meng Zhang *, Wei Zhou, Rongsheng Chen, Man Wong, Hoi-Sing Kwok

Center for Display Research and Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

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ABSTRACT

Water-enhanced degradation of p-type low temperature polycrystalline silicon thin film transistors under negative bias temperature (NBT) condition is studied. H_2O penetration into gate oxide network and the role of H_2O during NBT stress are confirmed and clarified respectively. To prevent H_2O diffusion, a combination of a layer of PECVD SiO_2 and a layer of PECVD Si_3N_4 as passivation layers are investigated, revealing that 100 nm SiO_2 and 300 nm Si_3N_4 can effectively block H_2O diffusion and improve device NBT reliability.

1. Introduction

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have attracted great research interest due to their applications in integrated active matrix displays [1]. To assure the performance of TFT based circuits, it is important to characterize the device intrinsic reliability and extrinsic instability induced by some parasitic effects. Negative bias temperature (NBT) instability (NBTI) has been widely studied in recent years and is found to be a key reliability issue for p-type LTPS TFTs [2,3], which is mainly attributed to the generation of interface/grain boundary (GB) trap states and fixed oxide charges. It is noted that among almost all NBTI studies in LTPS TFTs, the TFTs under test are without any passivation layers but only with a layer of low temperature oxide (LTO) as field oxide. These LTOs are usually deposited by either low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). These oxides are generally poor quality with porous structures [4]. Thus, one may doubt without any protection of additional passivation layers whether some parasitic effects are involved in NBT degradation.

In this work, water related parasitic effect in p-type LTPS TFTs under NBT stress is systematically studied. It is found that NBTI of polycrystalline silicon (poly-Si) TFTs without passivation layers is accelerated after 15 days' regular storing. By a series of experiments, it is confirmed that the enhanced NBTI is due to the H_2O penetration into gate oxide near the interface. The role of H_2O in the interface during NBT-stress is also clarified. To prevent such parasitic effect, different combinations of PECVD SiO_2 and PECVD Si_3N_4 passivation layers are applied on the top of poly-Si TFTs. The NBT stress test results reveal that 100 nm PECVD SiO_2 layer plus 300 nm PECVD Si_3N_4 layer can effectively keep H_2O from diffusing into the gate oxide network near interface and improve NBT reliability.

2. Experimental

TFTs used in this study were in conventional self-aligned top-gate structure as shown in Fig. 1. First, a layer of amorphous-Si (a-Si) was deposited on an oxidized silicon wafer by LPCVD. Then the a-Si layer is crystallized using either metal induced laterally crystallization (MILC) method [5] or solid phase crystallization (SPC) method [6]. After patterning of active islands, a 100 nm LTO layer was deposited as gate oxide, followed by sputtering of 300 nm pure Al as gate. After gate patterning, a self-aligned boron implantation with a dose of $4 \times 10^{15}\,cm^{-2}$ was done to form the source and drain. Then 500 nm LTO was deposited by LPCVD. Additional d_1 PECVD SiO_2 and d_2 PECVD Si_3N_4 were subsequently deposited, serving as passivation layers. Contact holes were opened before sputtering and patterning of Al–1% Si electrodes. Finally, wafers were sintered in forming gas at 420 °C for 30 min.

Typical NBT stress (stress $V_g = -25$ V with source/drain grounded) is applied to poly-Si TFTs with width (W)/length (L) = 10/10 μm. The wafer storage condition is in the air with 35% relative humidity at 25 °C. All thermal-humidity (T-H) treatments to the wafer are performed in the air with 95% relative humidity at 80 °C for 50 h and all the hard bake (H-B) treatments are carried out on a hot-plate at 150 °C for 15 h. Devices are measured before and after NBT stress by using Agilent 4156B semiconductor parameter analyzer at room temperature (25 °C). Degradation is characterized by analyzing the variation of threshold voltage (V_{th}) determined by the interception of linear extrapolation of a transfer curve at $V_{ds} = -0.1$ V.

* Corresponding author. Tel./fax: +852 2358 8845.
E-mail address: zhangmeng@ust.hk (M. Zhang).

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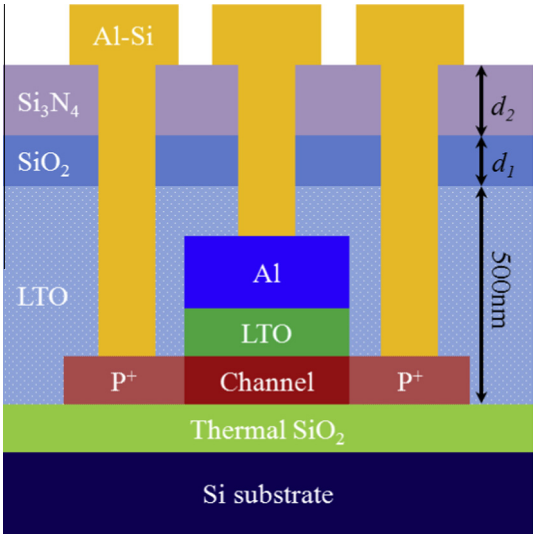

Fig. 1. The cross-sectional schematic diagram of a TFT used in the work. The d_1 and d_2 stands for the thickness of PECVD SiO_2 and PECVD Si_3N_4 respectively.

3. Results and discussion

The transfer curve degradation of a fresh MILC poly-Si TFT with $d_1 = d_2 = 0$ under NBT stress is shown in Fig. 2a. Evidently, typical NBTI degradation occurs. The V_{th} continuously shifts negatively while the subthreshold slope keeps almost constant [7]. The degradation slope (n) is 0.26 as shown in Fig. 2g, which is also consistent to that of typical NBTI degradation [2,7]. After 30,000 s stress, the V_{th} shifts about −0.32 V as shown in Fig. 2f. After the stress test, the wafer is kept in a dry box, in which the air has 35% relative humidity and the temperature is 25 °C. After 15 day storage, the same NBT stress is applied to another device with the same W/L = 10/10 μm. The degradation curve is shown in Fig. 2b. Compared to the fresh device as shown in Fig. 1a, the device after 15 days' storage suffers more serious NBTI degradation. The V_{th} shift after 30,000 s stress is more than −2.0 V as shown in Fig. 2f. Furthermore, the n is increased to 0.33 as shown in Fig. 2g. This significant difference between the two test results implies something may happen to the wafer during the wafer storage.

Since the test wafer does not have any additional passivation layers ($d_1 = d_2 = 0$), the H_2O in the air may penetrate the porous LTO structures into the gate oxide network and enhance NBTI. To verify the enhanced NBT degradation is related to the H_2O in the device structure, a series of experiments are designed and performed. First an H-B treatment is carried out on the wafer. When the wafer is cooled down to the room temperature after the H-B treatment, the same NBT stress test is performed on a TFT with the same W/L and the transfer curve degradation is shown in Fig. 2c. It is found that the NBTI is improved after the 15 h', H-B treatment. The shift after 30,000 s stress is recovered to about −1.0 V as shown in Fig. 2f and the n is decreased to 0.31 as shown in Fig. 2g. It is inferred that the H_2O in the device structure can be evaporated at high temperature and the NBTI is improved.

After the previous stress test, a T-H treatment is performed to the wafer immediately. During the T-H treatment, the H_2O diffusion into the gate oxide should be much more easily compared to that in the normal storage due to the higher air relative humidity plus higher temperature. After the T-H treatment, the wafer is quickly dried by employing N_2 gun. Again, the same NBT stress is applied to a TFT with the same W/L and the test result is shown in Fig. 2d. The NBTI is greatly deteriorated after the T-H treatment. The V_{th} shift is up to −4.1 V after 30,000 s stress as shown in Fig. 2f

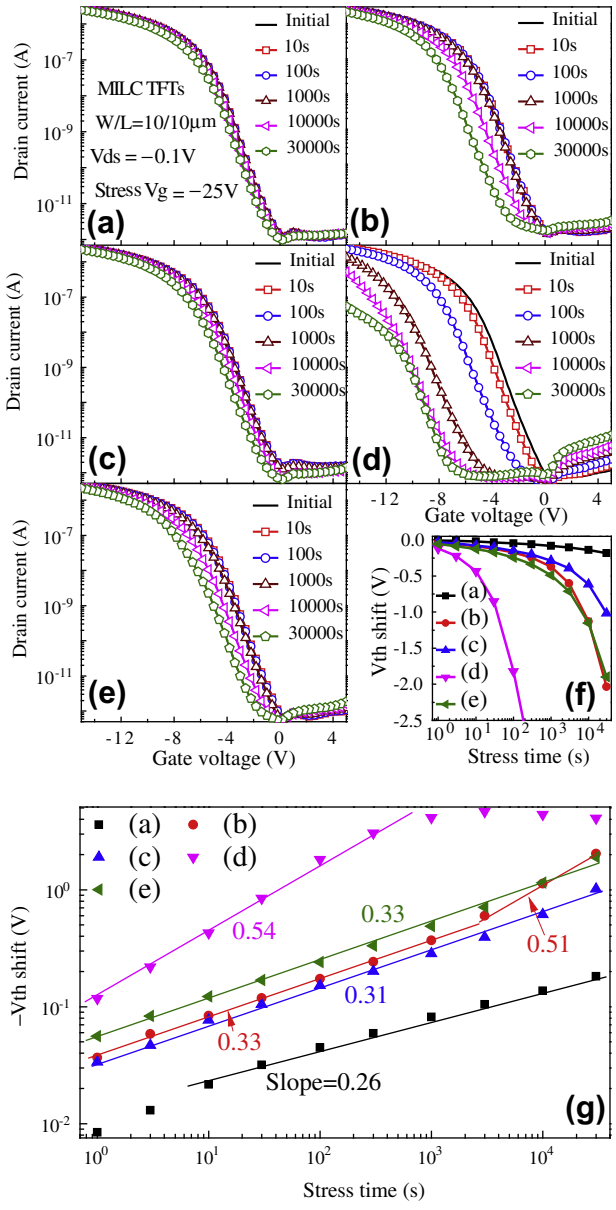

Fig. 2. (a–e): Time evolution of transfer characteristics under NBT stress for p-type MILC TFTs after a train of treatments. (a) A fresh TFT without any additional treatment. (b) A TFT after 15 days' normal storage. (c) A TFT after H-B treatment. (d) A TFT after T-H treatment. (e) A TFT after second round of H-B treatment following T-H treatment. (f): V_{th} shift dependent on stress time extracted from (a–e) plotted in semi-logarithmic scale. (g): V_{th} shift dependent on stress time extracted from (a–e) plotted in logarithmic scale.

and the n is dramatically increased to 0.54 as shown in Fig. 2g. It is believed the H_2O in the device structure enhances this NBTI. Finally, another H-B treatment to the wafer is performed after the above stress test. Consistent to the Fig. 2c, the NBTI of a TFT after the H-B treatment is greatly improved. The V_{th} shift is recovered from −4.1 V to −1.9 V as shown in Fig. 2f and the n is decreased from 0.54 to 0.33 as shown in Fig. 2g, due to the H_2O evaporation.

In LTPS TFTs, the NBT degradation is widely believed to be attributed to the generation of fixed charges and interface/GB trap states [2,3,7] without the consideration of H_2O effect. The water diffusion length in oxide [8,9] for 15 days' storage and for T-H treatment is estimated as 4.8 nm and 10.7 nm respectively, which are both much smaller than the field oxide thickness (500 nm). However, the experiment results indicate H_2O must diffuse into

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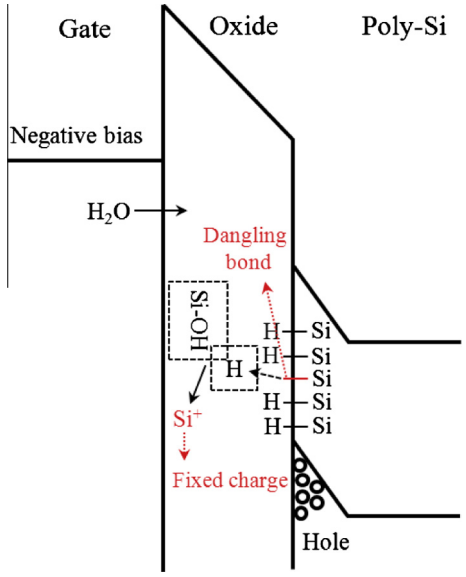

Fig. 3. Energy band diagram of p-type TFTs under NBT stress.

the device structure. Thus it can be inferred that the LPCVD field oxide much be porous and even have pinholes, which will shorten the water diffusion path. Only with this porous layer of field oxide as passivation layer, the H_2O will diffuse into the gate oxide network by a reaction [10]:

$$H_2O + \equiv Si{-}O{-}Si\equiv \leftrightarrow \equiv Si{-}OH + \equiv Si{-}OH.$$

As shown in Fig. 3, if "≡Si— H" at interface/GBs is activated by the high field, H^+ will be released from the "≡Si—H" [2], resulting in dangling bonds at interface/GBs. Then the released H^+ may react with the "≡Si—OH" nearby at the interface by

$$\equiv Si{-}OH + H^+ \leftrightarrow Si^+ + H_2O,$$

leading to positive fixed charge ($\equiv Si^+$) generation in the oxide at interface, enhancing NBT degradation. Based on the above experiment and discussion, it is thought that the factor of H_2O during the NBT stress should be taken into consideration.

To prevent the H_2O from diffusing into the gate oxide, different combinations of PECVD SiO_2 and PECVD Si_3N_4 passivation layers are applied on the top of LTPS TFTs. Shown in Fig. 4 is the dependence of V_{th} shift on stress time plotted in logarithmic scale for SPC poly-Si TFTs with different combinations of PECVD SiO_2 (d_1) and Si_3N_4 (d_2) passivation layers before and after T-H treatment. For the fresh TFT ($d_1 = d_2 = 0$) without T-H treatment and TFT ($d_1 = d_2 = 0$) with T-H treatment, the n are 0.281 and 0.540 respectively, consistent to that of MILC TFTs (Fig. 2a and d) discussed above. When depositing additional 100 nm PECVD SiO_2 (d_1 = 100 nm) as passivation layer, it is found that the n is reduced to 0.393 and the NBTI are greatly improved due to the better blockage of H_2O. When depositing another layer of PECVD Si_3N_4 (d_1 = 100 nm, d_2 = 100 nm), after T-H treatment, the n is continually reduced to 0.301 and the reliability is further improved, which is approaching to the intrinsic degradation of the fresh TFT. When increasing the d_2 to 300 nm and to 600 nm respectively, after the H-T treatment, the reliability is continually improved and the n is correspondingly decreased to 0.294 and to 0.281, which are nearly the same as intrinsic n (0.281) of the fresh TFT without the H-T treatment. By piling up different kinds of passivation layers (LPCVD SiO_2 + PECVD SiO_2 + PECVD Si_3N_4), the pinholes inside each porous layer could be shielded by each other, which will effectively keep the H_2O from diffusing into the gate oxide. On the other hand, PECVD oxide/nitride has smaller water diffusion coefficient than the LPCVD oxide [8,11]. Therefore depositing PECVD SiO_2 plus PECVD Si_3N_4 can also be effective in blocking H_2O diffusion.

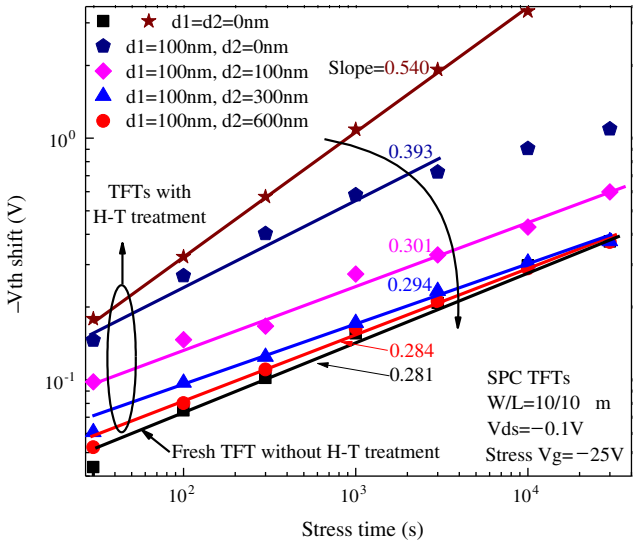

Fig. 4. Dependence of V_{th} shift on stress time for SPC TFTs with different combinations of PECVD SiO_2 and PECVD Si_3N_4 as passivation layers before and after T-H treatment, plotted in logarithmic scale.

4. Summary

Water-enhanced NBTI in p-type LTPS TFTs are investigated. H_2O diffusion into the device structure is confirmed by designing a series of experiments and the role of H_2O during NBT stress is clarified. Furthermore, to prevent H_2O from penetrating into the gate oxide network, different combinations of passivation layers are studied.

Acknowledgement

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